UTTARAKHAND TECHNICAL UNIVERSITY, DEHRADUN

M TECH (VLSI-Design) Programme
2018
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<thead>
<tr>
<th>Sr. No.</th>
<th>Type/Code</th>
<th>Course Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Core 1/ MVLT-101</td>
<td>Advance VLSI Design</td>
</tr>
<tr>
<td>2</td>
<td>Core 2/ MVLT-102</td>
<td>Advance VLSI Technology</td>
</tr>
<tr>
<td>3</td>
<td>Prog. Specific Elective PE1</td>
<td>Elective I</td>
</tr>
<tr>
<td></td>
<td>MVLT-111</td>
<td>(1) VLSI signal processing</td>
</tr>
<tr>
<td></td>
<td>MVLT-112</td>
<td>(2) CMOS RF Design</td>
</tr>
<tr>
<td></td>
<td>MVLT-113</td>
<td>(3) Network on chip design</td>
</tr>
<tr>
<td>4</td>
<td>Prog. Specific Elective PE2</td>
<td>Elective II</td>
</tr>
<tr>
<td></td>
<td>MVLT-121</td>
<td>(1) Advance Optical fiber communication</td>
</tr>
<tr>
<td></td>
<td>MVLT-122</td>
<td>(2) Designing with ASICs</td>
</tr>
<tr>
<td></td>
<td>MVLT-123</td>
<td>(3) Adv. Digital communication</td>
</tr>
<tr>
<td>5</td>
<td>LAB 1/ MVLP-101</td>
<td>VLSI circuit Design lab</td>
</tr>
<tr>
<td>6</td>
<td>LAB 2/ MVLP-102</td>
<td>VLSI signal processing lab (MATLAB)</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>Research Methodology and IPR</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>Audit course 1</td>
</tr>
</tbody>
</table>

Semester-II

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Type/Code</th>
<th>Course Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Core 3/ MVLT-201</td>
<td>CAD using VLSI system Design</td>
</tr>
<tr>
<td>2</td>
<td>Core 4/ MVLT-202</td>
<td>Algorithm for VLSI Physical Design automation</td>
</tr>
<tr>
<td>3</td>
<td>Prog. Specific Elective PE3</td>
<td>Elective III</td>
</tr>
<tr>
<td></td>
<td>MVLT-231</td>
<td>(1) CMOS analog circuit Design</td>
</tr>
<tr>
<td></td>
<td>MVLT-232</td>
<td>(2) Memory Technology</td>
</tr>
<tr>
<td></td>
<td>MVLT-233</td>
<td>(3) SOC Design</td>
</tr>
<tr>
<td>4</td>
<td>Prog. Specific Elective PE2</td>
<td>Elective IV</td>
</tr>
<tr>
<td></td>
<td>MVLT-241</td>
<td>(1) Low power VLSI Design</td>
</tr>
<tr>
<td>Sr. No.</td>
<td>Course Type/Code</td>
<td>Course Name</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------</td>
<td>------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>Prog. Specific Elective PE5</td>
<td>(1) Testing of VLSI circuit</td>
</tr>
<tr>
<td></td>
<td>MVLT-351</td>
<td>(2) Nano materials and Nanotechnology</td>
</tr>
<tr>
<td></td>
<td>MVLT-353</td>
<td>(3) FPGA architecture and application</td>
</tr>
<tr>
<td>2</td>
<td>Open Elective / MVLT-591</td>
<td>1. Business Analytics</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Industrial Safety</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. Operations Research</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5. Composite Materials</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6. Waste to Energy</td>
</tr>
<tr>
<td>3</td>
<td>Dissertation / MVLP-301</td>
<td>Dissertation Phase – I</td>
</tr>
</tbody>
</table>

### Semester-IV

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Course Type/Code</th>
<th>Course Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Dissertation / MVLP-401</td>
<td>Dissertation Phase – II</td>
</tr>
</tbody>
</table>

**Audit course 1 & 2**
- English for Research Paper Writing
- Disaster Management
- Sanskrit for Technical Knowledge
- Value Education
- Constitution of India
- Pedagogy Studies
- Stress Management by Yoga
<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Course Type/Code</th>
<th>Course Name</th>
<th>Teaching Scheme</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td>L</td>
<td>T</td>
</tr>
<tr>
<td>1</td>
<td>Core 1/</td>
<td>Advance VLSI Design</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLT-101</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Core 2/</td>
<td>Advance VLSI technology</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLT-102</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Prog. Specific</td>
<td>Elective I</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Elective PE1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-111</td>
<td>(1) VLSI signal processing</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-112</td>
<td>(2) CMOS RF Design</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-113</td>
<td>(3) Network on chip design</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Prog. Specific</td>
<td>Elective II</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Elective PE2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-121</td>
<td>(1) Advance Optical fiber communication</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-122</td>
<td>(2) Designing with ASICs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-123</td>
<td>(3) Adv. Digital communication</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>LAB 1/</td>
<td>VLSI circuit Design lab</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLP-101</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>LAB 2/</td>
<td>VLSI signal processing lab (MATLAB)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLP-102</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>Research Methodology and IPR</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>Aud 1</td>
<td>Audit course 1</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td><strong>Total</strong></td>
<td>16</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Course Type/Code</th>
<th>Course Name</th>
<th>Teaching Scheme</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
</tr>
<tr>
<td>1</td>
<td>Core 3/</td>
<td>CAD using VLSI system Design</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLT-201</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Core 4/</td>
<td>Algorithm for VLSI Physical Design automation</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLT-202</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Prog. Specific</td>
<td>Elective III</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Elective PE3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-231</td>
<td>(1) CMOS analog circuit Design</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-232</td>
<td>(2) Memory Technology</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-233</td>
<td>(3) SOC Design</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sr. No.</td>
<td>Course Type/Code</td>
<td>Course Name</td>
<td>Teaching Scheme</td>
<td>Credits</td>
</tr>
<tr>
<td>--------</td>
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<td>----------------------------------</td>
<td>-----------------</td>
<td>---------</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
</tr>
<tr>
<td>4</td>
<td>Prog. Specific</td>
<td>Elective IV</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Elective PE2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-241</td>
<td>(1) Low power VLSI Design</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLT-242</td>
<td>(2) Memory Technologies</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLT-243</td>
<td>(3) Hardware software codesign</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>LAB 3/</td>
<td>FPGA Design Lab</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLP-201</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>LAB 4/</td>
<td>TCAD Lab</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLP-202</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>MVLP-203</td>
<td>Seminar</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>Aud 2</td>
<td>Audit course 2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>Total</td>
<td></td>
<td>14</td>
<td>0</td>
</tr>
</tbody>
</table>

**Semester-III**

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Course Type/Code</th>
<th>Course Name</th>
<th>Teaching Scheme</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
</tr>
<tr>
<td>1</td>
<td>Prog. Specific</td>
<td>Elective V</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Elective PE5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MVLT-351</td>
<td>(1) Testing of VLSI circuit</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLT-352</td>
<td>(2) Nano materials and Nanotechnology</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLT-353</td>
<td>(3) FPGA architecture and application</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>Open Elective /</td>
<td>1. Business Analytics</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLT-391</td>
<td>2. Industrial Safety</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. Operations Research</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. Cost Management of Engineering Projects</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5. Composite Materials</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6. Waste to Energy</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Dissertation /</td>
<td>Dissertation Phase – I</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MVLP-301</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Total</td>
<td></td>
<td>6</td>
<td>0</td>
</tr>
</tbody>
</table>

**Semester-IV**

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Course Type/Code</th>
<th>Course Name</th>
<th>Teaching Scheme</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td>L</td>
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</tr>
<tr>
<td>1</td>
<td>Dissertation /</td>
<td>Dissertation Phase – II</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td></td>
<td>MVLP-401</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Total</td>
<td></td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>
Audit course 1 & 2

1. for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
Unit 1
Introduction: Basic principle of MOS transistor, Introduction to large signal MOS models (long channel) for digital design.

MOS Circuit Layout & Simulation and manufacturing: scaling, MOS SPICE model and simulation, CMOS Layout: design rules, Transistor layout, Inverter layout, NMOS and CMOS basic manufacturing steps.

Unit 2
The MOS Inverter: Inverter principle, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, switching characteristics, Propagation Delay, Power Consumption.

Combinational MOS Logic Design: Static MOS design, Ratioed logic, Pass Transistor logic, complex logic circuits.

Unit 3
Sequential MOS Logic Design
Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Astable Circuits.
Memory Design: ROM & RAM cells design
Dynamic MOS design: Dynamic logic families and performances.
Clock Distribution: Clock Distribution. Input and Output Interface circuits.

Unit 4
Subsystem design
Design styles, design concepts: Hierarchy, Regularity, Modularity, Locality. CMOS Sub system design: Adders, Multipliers.

Text Books

Reference Books
Neil Weste and David Harris :“ CMOS VLSI design” Pearson Education 2009.
Unit 1
Cleanroom technology - Clean room concept – Growth of single crystal Si, surface contamination, Chemical Mechanical Polishing, wafer preparation, DI water, RCA and Chemical Cleaning. Processing considerations: Chemical cleaning, getting the thermal Stress factors etc.

Epitaxy : Physical Vapour Deposition, Vapors phase Epitaxy Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

Unit 2
Diffusion : Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source, Ion Implantation, Annealing and diffusion from an ion implanted layer.

Unit 3
Lithography

Unit 4
Etching
Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching. Metallisation - Different types of metallization, uses & desired properties

Text Books

Reference Books
Subject: ADVANCED VLSI SIGNAL PROCESSING

Unit I

Unit II

Unit III
Frequency Domain Realization of Digital Filters, Radix-2 FFT Algorithm. Introduction to Multirate digital signal processing

Unit IV

Text:

Reference:
Paper : CMOS RF DESIGN

Unit 1


Unit 2


Unit 3


Unit 4


Text Books


Reference Books:

Unit 1


Unit 2


Unit 3


Unit 4


Text Books:

Reference Books:
[R3] Giovanni De Micheli, Luca Benini, Networks on Chips: Technology and Tools (Systems on Silicon), Morgan Kaufmann; 1 edition (August 3, 2006)
Paper: Advance optical fiber communication

Unit 1

Introduction to optical communication: principle of transmission, optical fiber modes and configuration mode theory for circular waveguides, single mode fiber, multimode fiber, numerical aperture, mode field diameter, fiber fabrication techniques.

Unit 2

Optical source LED, LASER Diodes, modal reflection noise, power launching and coupling, populations, fiber splicing, optical connector, photo detector PIN, Avalanche detector, response time, avalanche multiplication noise

Unit 3

Signal degradation in optical fiber, attenuation losses, signal distortion optical waveguide dispersion, chromatic dispersion, and pulse broadening in graded index fibers, mode coupling advanced fiber design, dispersion shifted, dispersion compensating fiber, design optimization of single mode fibers.

Unit 5

Coherent optical fiber communication, modulation techniques, misalignment, fiber to fiber joints, optical fiber link design, rise time budget and link power budget, long haul system, bit error rate, line coding: NRZ, RZ, Block code, error code, error corrections.

Unit 6

WDM concepts and components, operation, fiber granting, hologram, tunable filter, directional couple, dispersion managements, optical amplifier –EDFA, photonic switching, optical network – SONET / SDH, optical interference, ring topology, star architecture.

REFERENCES:

- D.Mynbav and Scheiner , “fiber optical communication technology “, PHI.
Paper Code No : MVLT-122

Paper – DESIGNING WITH ASICS

Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.

ASIC Library design: Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC

Low level design entry: Schematic entry – low level design languages – PLA tools – EDIF – An overview of VHDL and verilog. Logic synthesis in verilog and & VHDL simulation.

ASIC Construction – Floor planning & placement – Routing.

Text / References:

Unit 1: Modulation Techniques

Digital Modulation Techniques - Analysis, Generation and Detection (Block Diagram), Spectrum and Bandwidth of Amplitude Shift Keying (ASK), Binary Phase Shift Keying (BPSK), Differential Phase Shift Keying (DPSK), Offset and Non-offset Quadrature Phase Shift Keying (QPSK), M-ary PSK, Binary Frequency Shift Keying (BFSK), M-ary FSK, Minimum Shift Keying, Quadrature Amplitude Modulation (QAM), Comparison of digital modulation techniques on the basis of probability of error, Matched Filter.

Unit 2: Pulse Modulation

Sampling of Signal, Sampling Theorem for Low Pass and Band Pass Signals, Aliasing, Pulse Amplitude Modulation (PAM), Time Division Multiplexing (TDM), Channel Bandwidth for PAM-TDM Signal, Types of Sampling, Instantaneous, Natural and Flat Top Sampling, Aperture Effect, PPM and PDM techniques, Pulse Code Modulation (PCM), Signal-to-Noise Ratio in PCM, Companding, Data Rate and Bandwidth of Multiplexed PCM Signal, Inter-symbol Interference, Eye Diagram, Line Coding NRZ, RZ, Biphasic, Differential PCM (DPCM), Delta Modulation (DM), and Adaptive Delta Modulation (ADM), Slope Overload Error, Granular Noise, Comparison of various system in terms of Bandwidth and Signal-to-Noise Ratio.

Unit 3: Random Processes


Unit 4: Spread Spectrum Modulation

Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum with coherent binary phase shift keying, signal space dimensionality and processing gain, probability of error, frequency hop spread spectrum, maximum length and Golay codes.

Text Books:
[T1] B. Sklar, Digital Communication, Pearson Education.

References:
[R1] Taub & Schilling, Principles of Communication system, TMH.
[R5] Schaum’s Outline series, Analog and Digital Communication.
[R7] Couch: Digital and Analog Communication, Pearson Education
UNIT 1

(i) **Introduction**: Evolution of design automation; CMOS realization of basic gates.

(ii) **Circuit and system representation**: Behavioral, structural and physical models, design flow.

UNIT 2

(i) **Modeling techniques**: Type of CAD tools, introduction to logic simulation and synthesis.

(ii) **HDL**: syntax, hierarchical modeling, verilog construct, simulator directives, instantiating modules, gate level modeling.

UNIT 3

(i) **DELAY MODELING**: Event based and level sensitive timing control memory initialization, conditional compilation time scales for simulation.

(ii) **Advanced modeling techniques**: Static timing analysis, delay, switch level modeling, user defined primitive (UDP), memory modeling.

UNIT 4

(i) **Logic synthesis**: Logic synthesis of HDL, constructs, cell library, design constraints, synthesis design flow.

(ii) **Advanced verification techniques**: Traditional verification flow, Architectural modeling Assertion checking, formal verification.

UNIT 5

(i) **FPGAs based system design**: Commercial FPGA architecture LUT and routing architecture, FPGA CAD flow.

Name of Authors/Books/Publishers

VLSI physical design automation and Fabrication: VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices

**VLSI automation Algorithms Partitioning:** Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing.

**Floor planning & pin assignment:** Problem formulation, classification of floorplanning algorithms, constraint based floor planning, floor planning algorithms for mixedblock\& cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment Placement Problem formulation, classification of placement algorithms, simulation base placement algorithms, recent trends in placement

**Global Routing and Detailed routing:** Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms.

**Over the cell routing & via minimization:** Two layers over the cell routers, constrained & unconstrained via minimization

**Compaction:** Problem formulation, classification of compaction algorithms, one dimensional compaction, two dimension based compaction, hierarchical compaction

**Reference Books:**

UNIT I

UNIT II
**Single-Stage Amplifiers**, Basic Concepts, Common-Source Stage, Common-Source Stage with Resistive Load, CS Stage with Diode-Connected Load, CS Stage with Current-Source Load, CS Stage with Triode Load, CS Stage with Source Degeneration, Source Follower, Common-Gate Stage, Cascode Stage, Folded Cascode, Choice of Device Models.

UNIT III

UNIT IV

UNIT V

Reference Books:
Paper Code: MVLT-232

**Paper – MEMORY TECHNOLOGIES**

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOI, Advanced SRAM Architectures, Application Specific SRAMs; DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM.

Non-Volatile Memories: High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories.


Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.

**Reference Books:**


Hardware-Software codesign, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc.

Embedded Memories –cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence.MESI protocol and Directory-based coherence.


MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design

Case Study: A Low Power Open Multimedia Application Platform for 3G and 4G Wireless Communication Technology.

Text Books:

MTVL101 – LOW POWER VLSI DESIGN

UNIT I: LOW POWER DESIGN, AN OVERVIEW: Introduction to low-voltage low power design, limitations, Silicon-on-Insulator.


UNIT IV: DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT V: CMOS AND BI-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

UNIT VI: LOW-VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.


UNIT VIII: SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Text Books:
1. Yeo Rofail/ Gohl, CMOS/BiCMOS ULSI low voltage, low power, PearsonEducation.
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP.
5. Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, TMH Publication.
Paper Code: MVLT-2433
Paper: HARDWARE/SOFTWARE CODESIGN

Unit 1

Introduction [T1]: Motivation hardware & software co-design, system design consideration, research scope overviews. Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance modeling, Hardware Software development.

Unit 2

Hardware Software co-design research[T1]: An informal view of co-design, Hardware Software tradeoffs, crosses fertilization, typical co- design process, co-design environments, limitation of existing approaches, ADEPT modeling environment. Co-design concepts: Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software trade offs, co-design.

Unit 3

Methodology for co-design[T1]: Amount of unification, general consideration & basic philosophies, a framework for co-design. Unified representation for Hardware & Software : Benefits of unified representation, modeling concepts. An abstract Hardware & Software model : Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model.

Unit 4

Performance evaluation[T1]: Application of the abstract Hardware & Software model, examples of performance evaluation. Object oriented techniques in hardware design: Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, Processor example.

Text Books:


Reference Books:

UNIT I - BASICS OF TESTING AND FAULT MODELING
Introduction - Principle of testing - types of testing - DC and AC parametric tests - fault modeling
- Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation

UNIT II - TESTING AND TESTABILITY OF COMBINATIONAL CIRCUITS
Test generation basics - test generation algorithms - path sensitization - Boolean difference – D-algorithm – PODEM
- Testable combinational logic circuit design.

UNIT III - TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS
Testing of sequential circuits as iterative combinational circuits - state table verification - test generation based on
circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) -
partial scan - Boundary scan

UNIT IV - MEMORY, DELAY FAULT AND IDDQ TESTING
Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults - Delay test- IDDQ testing
- testing methods - limitations of IDDQ Testing

UNIT V - BUILT-IN SELF-TEST
Test pattern generation of Built-in Self-Test (BIST) - Output response analysis – BIST architectures.

Reference Books:
   Springer.
Elective IV

Paper Code: MVLT-352

Paper: Nano materials and Nanotechnology

Course Outcomes:
At the end of the course, students will be able to:

CO1: To understand the basic science behind the design and fabrication of nano scale systems.
CO2: To understand and formulate new engineering solutions for current problems and competing technologies for future applications.
CO3: To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
CO4: To gather detailed knowledge of the operation of fabrication and characterisation devices to achieve precisely designed systems.

Syllabus Contents:

Unit 1: Nanomaterials in one and higher dimensions,

Unit 2: Applications of one and higher dimension nano-materials.

Unit 3: Nano-lithography, micro electro-mechanical system (MEMS) and nano-phonics.

Unit 4: Carbon nanotubes – synthesis and applications

Unit 5 and 6: Interdisciplinary arena of nanotechnology.

References:

UNIT-I

Programmable Logic ROM, PLA, PAL, PLD, PGA–Features, programming and applications using complex programmable logic devices Altera series–Max 5000/7000 series and Altera FLEX logic–10000 series CPLD, AMD’s–CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST’s Architectures–3000 Series–Speed Performance and in system programmability.

UNIT-II

FPGAs Field Programmable Gate Arrays–Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs.

UNIT-III

Case Studies Xilinx XC4000 & ALTERA’s FLEX 8000/10000 FPGAs: AT &T–ORCA’s (Optimized Reconfigurable Cell Array): ACTEL’s–ACT-1,2,3 and their speed performance. UNIT-IV
Finite State Machines (FSM)-I Top-down Design–State Transition Table, state assignments for FPGAs, Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL.

UNIT-V


UNIT-VI

FSM Architectures and Systems Level Design Architectures centered around non-registered PLDs, State machine designs centered around shift registers, One–Hot design method, Use of ASM’s in One–Hot design. K Application of One–Hot method, System level design controller, data path and functional partition.

UNIT-VII


UNIT-VIII

Guidelines and Case Studies Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

Reference Books:
Teaching Scheme: Lab
20 and 30 Hrs/Week

Course Outcomes:
At the end of this course, students will be able to
   Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem.
   Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
   Ability to present the findings of their technical solution in a written report. Presenting the work in International/ National conference or reputed journals.

Syllabus Contents:
The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following
Relevance to social needs of society
Relevance to value addition to existing facilities in the institute
Relevance to industry need
Problems of national importance
Research and development in various domain

Literature survey Problem Definition
Motivation for study and Objectives
Preliminary design / feasibility / modular approaches
Implementation and Verification

Report and presentation

The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification / Proof of concept.
- Design, fabrication, testing of Communication System.
- The viva-voce examination will be based on the above report and work.


As per the AICTE directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June. The dissertation may be carried out preferably in-house i.e. department’s laboratories and centers OR in industry allotted through department’s T & P coordinator.

After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.

Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.

Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.

Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.

During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.

Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, a record of continuous progress.

Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q & A. In case of
OPEN ELECTIVES
Business Analytics

Teaching scheme
Lecture: - 3 h/week

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Name</th>
<th>Credits</th>
<th>Prerequisites</th>
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<tr>
<td></td>
<td>Business Analytics</td>
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Total Number of Lectures: 48

Course objective

Understand the role of business analytics within an organization.
Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization.
To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making.
To become familiar with processes needed to develop, report, and analyze business data.
Use decision-making tools/Operations research techniques.
Manage business process using analytical and management tools.
Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.

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<thead>
<tr>
<th>LECTURE WITH BREAKUP</th>
<th>NO. OF LECTURES</th>
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<tr>
<td><strong>Unit 1:</strong></td>
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<td><strong>Unit 2:</strong></td>
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<tr>
<td>Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.</td>
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<tr>
<td><strong>Unit 3:</strong></td>
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<tr>
<td>Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling,</td>
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<tr>
<td>Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.</td>
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<td><strong>Unit 5:</strong> Decision Analysis: Formulating Decision Problems, Decision 8 Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.</td>
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<td><strong>Unit 6:</strong> Recent Trends in : Embedded and collaborative business intelligence, 4 Visual data recovery, Data Storytelling and Data journalism.</td>
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<tr>
<td><strong>COURSE OUTCOMES</strong></td>
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</table>
| Students will demonstrate knowledge of data analytics.  
Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.  
Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making.  
Students will demonstrate the ability to translate data into clear, actionable insights. |
| **Reference:**  
Business Analytics by James Evans, persons Education. |

**OPEN ELECTIVES**  
**Industrial Safety**  
Lecture: - 3 h/week  
**Unit-I:** Industrial safety: Accident, causes, types, results and control, mechanical and electricalhazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.  
**Unit-II:** Fundamentals of maintenance engineering: Definition and aim of maintenance engineering,Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Unit-IV: Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment’s like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

Unit-V: Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Reference:
Maintenance Engineering, H. P. Garg, S. Chand and Company.

OPEN ELECTIVES
Operations Research

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes: At the end of the course, the student should be able to

Students should able to apply the dynamic programming to solve problems of discreet and continuous variables.
Students should able to apply the concept of non-linear programming
Students should able to carry out sensitivity analysis
Student should able to model the real world problem and simulate it.

Syllabus Contents:

Unit 1:
Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

Unit 2:
Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

Unit 3:
Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT
Unit 4
Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit 5
Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

References:
J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
Pannerselvam, Operations Research: Prentice Hall of India 2010

Open Elective
Cost Management of Engineering Projects

Teaching scheme
Lecture: - 3 h/week

Introduction and Overview of the Strategic Cost Management Process

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non-technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process


References:
- Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
- Charles T. Horngren and George Foster, Advanced Management Accounting
- Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
- N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.


UNIT – V: Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS:

References:

Open Elective
Waste to Energy

Teaching scheme
Lecture: - 3 h/week


thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

**Unit-IV:** Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

**Unit-V:** Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

**References:**


**AUDIT 1 and 2: ENGLISH FOR RESEARCH PAPER WRITING**

**Course objectives:**

Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title

<table>
<thead>
<tr>
<th>Units</th>
<th>CONTENTS</th>
<th>Hours</th>
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<tbody>
<tr>
<td>1</td>
<td>Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness</td>
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<tr>
<td>3</td>
<td>Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.</td>
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<tr>
<td>4</td>
<td>key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions</td>
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<tr>
<td>6</td>
<td>useful phrases, how to ensure paper is as good as it could possibly be the first-time submission</td>
<td>4</td>
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</table>

**Suggested Studies:**

AUDIT 1 and 2: DISASTER MANAGEMENT

Course Objectives: Students will be able to:

- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Syllabus

<table>
<thead>
<tr>
<th>Units</th>
<th>CONTENTS</th>
<th>Hours</th>
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<tbody>
<tr>
<td>1</td>
<td><strong>Introduction</strong>&lt;br&gt;Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.</td>
<td>4</td>
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<td>3</td>
<td><strong>Repercussions Of Disasters And Hazards</strong>: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Manmade disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.</td>
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<td>4</td>
<td><strong>Disaster Prone Areas In India</strong>&lt;br&gt;Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics</td>
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<td>5</td>
<td><strong>Disaster Preparedness And Management</strong>&lt;br&gt;Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.</td>
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<td>6</td>
<td><strong>Disaster Mitigation</strong>&lt;br&gt;Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.</td>
<td>4</td>
</tr>
</tbody>
</table>
SUGGESTED READINGS:
Sahni, PardeepEt.Al. (Eds.),” Disaster Mitigation Experiences And Reflections”, Prentice Hall Of India, New Delhi.

AUDIT 1 and 2: SANSKRIT FOR TECHNICAL KNOWLEDGE

Course Objectives
To get a working knowledge in illustrious Sanskrit, the scientific language in the world
Learning of Sanskrit to improve brain functioning
Learning of Sanskrit to develop the logic in mathematics, science & other subjects
enhancing the memory power
The engineering scholars equipped with Sanskrit will be able to explore
the huge knowledge from ancient literature

Syllabus

<table>
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<tr>
<th>Unit</th>
<th>Content</th>
<th>Hours</th>
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<tbody>
<tr>
<td>1</td>
<td>Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences</td>
<td>8</td>
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<tr>
<td>2</td>
<td>Order Introduction of roots Technical information about Sanskrit Literature</td>
<td>8</td>
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<tr>
<td>3</td>
<td>Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics</td>
<td>8</td>
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Suggested reading
“Abhyaspustakam” – Dr. Vishwas, Sanskrita-Bharti Publication, New Delhi
“Teach Yourself Sanskrit” PrathamaDeeksha-VempatiKutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
“India’s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd., New Delhi.

Course Output
Students will be able to
Understanding basic Sanskrit language
Ancient Sanskrit literature about science & technology can be understood
Being a logical language will help to develop logic in students

AUDIT 1 and 2: VALUE EDUCATION

Course Objectives
Students will be able to
1. Understand value of education and self- development
2. Imbibe good values in students
Let the should know about the importance of character

**Syllabus**

<table>
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<tr>
<th>Unit</th>
<th>Content</th>
<th>Hours</th>
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<tbody>
<tr>
<td>1</td>
<td>Values and self-development –Social values and individual attitudes.</td>
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<td></td>
<td>Work ethics, Indian vision of humanism.</td>
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<td></td>
<td>Moral and non- moral valuation. Standards and principles.</td>
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<td>Value judgements</td>
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<td>2</td>
<td>Importance of cultivation of values.</td>
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<td></td>
<td>Sense of duty. Devotion, Self-reliance.</td>
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<td></td>
<td>Truthfulness, Cleanliness.</td>
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<td>Honesty, Humanity. Power of faith, National Unity.</td>
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<td>Patriotism. Love for nature, Discipline</td>
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<td>3</td>
<td>Personality and Behavior Development - Soul and Scientific attitude.</td>
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<td>Positive Thinking, Integrity and discipline.</td>
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<td>Punctuality, Love and Kindness.</td>
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<td>Avoid fault Thinking.</td>
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<td>Free from anger, Dignity of labour.</td>
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<td>Universal brotherhood and religious tolerance.</td>
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<td>True friendship.</td>
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<td>Happiness Vs suffering, love for truth.</td>
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<td>Aware of self-destructive habits.</td>
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<td>Association and Cooperation.</td>
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<td>Doing best for saving nature.</td>
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<td>4</td>
<td>Character and Competence –Holy books vs Blind faith.</td>
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<td></td>
<td>Self-management and Good health.</td>
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<td>Science of reincarnation.</td>
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<td>Equality, Nonviolence, Humility, Role of Women.</td>
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<td>All religions and same message.</td>
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<td>Mind your Mind, Self-control.</td>
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<td></td>
<td>Honesty, Studying effectively</td>
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</table>

**Suggested reading**
1 Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

**Course outcomes**
Students will be able to
1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

**AUDIT 1 and 2: CONSTITUTION OF INDIA**
**Course Objectives:**

Students will be able to:
- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

### Syllabus

<table>
<thead>
<tr>
<th>Units</th>
<th>Content</th>
<th>Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1</strong></td>
<td>History of Making of the Indian Constitution: Drafting Committee, (Composition &amp; Working)</td>
<td>4</td>
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<tr>
<td><strong>2</strong></td>
<td>Philosophy of the Indian Constitution: Preamble Salient Features</td>
<td>4</td>
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<tr>
<td><strong>3</strong></td>
<td>Contours of Constitutional Rights &amp; Duties: Fundamental Rights Right to Equality Right to Freedom Right against Exploitation Right to Freedom of Religion Cultural and Educational Rights Right to Constitutional Remedies Directive Principles of State Policy Fundamental Duties.</td>
<td>4</td>
</tr>
<tr>
<td><strong>4</strong></td>
<td>Organs of Governance: Parliament Composition Qualifications and Disqualifications Powers and Functions Executive President Governor Council of Ministers Judiciary, Appointment and Transfer of Judges, Qualifications Powers and Functions</td>
<td>4</td>
</tr>
</tbody>
</table>
Local Administration:
District’s Administration head: Role and Importance,
Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation.
Elected officials and their roles, CEO ZilaPachayat: Position and role.
Block level: Organizational Hierarchy (Different departments),
Village level: Role of Elected and Appointed officials,
Importance of grass root democracy

Election Commission:
Election Commission: Role and Functioning.
Chief Election Commissioner and Election Commissioners.
State Election Commission: Role and Functioning.
Institute and Bodies for the welfare of SC/ST/OBC and women.

Suggested reading
The Constitution of India, 1950 (Bare Act), Government Publication.

Course Outcomes:
Students will be able to:
Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
Discuss the passage of the Hindu Code Bill of 1956.

AUDIT 1 and 2: PEDAGOGY STUDIES

Course Objectives:
Students will be able to:
Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
Identify critical evidence gaps to guide the development.

<table>
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<tr>
<th>Syllabus</th>
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<tbody>
<tr>
<td>Units</td>
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<tr>
<td>1</td>
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<td>3</td>
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<tr>
<td>4</td>
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<tr>
<td><strong>Research gaps and future directions</strong></td>
</tr>
</tbody>
</table>
- Research design  
- Contexts  
- Pedagogy  
- Teacher education  
- Curriculum and assessment  
- Dissemination and research impact. |
| 5 | |

**Suggested reading**


**Course Outcomes:**

Students will be able to understand:

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?

How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

AUDIT 1 and 2: STRESS MANAGEMENT BY YOGA

Course Objectives
To achieve overall health of body and mind
To overcome stress

Syllabus

<table>
<thead>
<tr>
<th>Unit</th>
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<tbody>
<tr>
<td>1</td>
<td>Definitions of Eight parts of yog. (Ashtanga)</td>
<td>8</td>
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<tr>
<td>2</td>
<td>Yam and Niyam. Do’s and Don't's in life.</td>
<td>8</td>
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<tr>
<td></td>
<td>i) Ahinsa, satya, astheya, bramhacharya and aparigraha</td>
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<tr>
<td></td>
<td>ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan</td>
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<tr>
<td>3</td>
<td>Asan and Pranayam</td>
<td>8</td>
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<tr>
<td></td>
<td>i) Various yog poses and their benefits for mind &amp; body</td>
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<td></td>
<td>ii) Regularization of breathing techniques and its effects - Types of</td>
<td></td>
</tr>
<tr>
<td></td>
<td>pranayam</td>
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</tbody>
</table>

Suggested reading
‘Yogic Asanas for Group Training-Part-I’ : Janardan Swami YogabhyasiMandal, Nagpur
“Rajayoga or conquering the Internal Nature” by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

Course Outcomes:
Students will be able to:
- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

AUDIT 1 and 2: PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

Course Objectives
To learn to achieve the highest goal happily
To become a person with stable mind, pleasing personality and determination
To awaken wisdom in students

Syllabus

<table>
<thead>
<tr>
<th>Unit</th>
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<tbody>
<tr>
<td>1</td>
<td>Neetisatakam-Holistic development of personality</td>
<td>8</td>
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<td></td>
<td>Verses- 19,20,21,22 (wisdom)</td>
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<td>Verses- 29,31,32 (pride &amp; heroism)</td>
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<td>Verses- 26,28,63,65 (virtue)</td>
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<td>Verses- 52,53,59 (dons)</td>
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<tr>
<td></td>
<td>Verses- 71,73,75,78 (dos)</td>
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</tbody>
</table>
| 2 | Approach to day to day work and duties.  
ShrimadBhagwadGeeta : Chapter 2-Verses 41, 47, 48, 
Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5, 13, 17, 
23, 35, 
Chapter 18-Verses 45, 46, 48. | 8 |

| 3 | Statements of basic knowledge.  
ShrimadBhagwadGeeta: Chapter2-Verses 56, 62, 68  
Chapter 12 -Verses 13, 14, 15, 16, 17, 18  
Personality of Role model. ShrimadBhagwadGeeta:  
Chapter2-Verses 17, Chapter 3-Verses 36, 37, 42,  
Chapter 4-Verses 18, 38, 39  
Chapter18 – Verses 37, 38, 63 | 8 |

**Suggested reading**

“Srimad Bhagavad Gita” by Swami SwarupanandaAdvaita Ashram  
(Publication Department), Kolkata  
Bhartrihari’s Three Satakam (Niti-sringar-vairagya) by  
P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

**Course Outcomes**

Students will be able to  
Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life  
The person who has studied Geeta will lead the nation and mankind to peace and prosperity  
Study of Neetishatakam will help in developing versatile personality of students.