SYLLABUS

For

Master of Engineering Programmes

(M.Tech. VLSI DESIGN)

(For admission in 2022-23 and onwards)
# Courses Structure and Scheme of Examination for M. Tech.- 2 Year Programme

## VLSI Design

### Semester I

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Course Type/Code</th>
<th>Course Name</th>
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<td>CT</td>
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<td>VDT301</td>
<td>CMOS Analog Circuit Design</td>
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**Total**

### Professional Elective-I

- (4) Low Power VLSI Design
- (5) System on Chip Design
- (6) VLSI Signal Processing

### Professional Elective-II

- (7) Mixed Signal IC Design
- (8) Memory Technologies
- (9) Hardware and Software Co-Design

### Open Elective(Optional)

- (1) IoT and its Applications
- (2) Artificial Intelligence and Machine Learning
- (3) Composite Materials
- (4) Industrial Safety
- (5) Non-Conventional Energy Sources

### Semester II (M. Tech.- 2 Year Programme)

<table>
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<th>Sr. No.</th>
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### Professional Elective-III
- (2) Embedded System Design
- (3) Testing of VLSI Circuits
- (4) ASIC Design ESIGN Using Verilog

### Professional Elective-IV
- (5) Algorithms for VLSI Design Automation
- (6) Sensors and Actuators
- (7) Design for Testability

### Open Elective-2
- (1) IoT and its Applications
- (2) Artificial Intelligence and Machine Learning
- (3) Composite Materials
- (4) Industrial Safety
- (5) Non-Conventional Energy Sources

### Semester III(M. Tech.- 2 Year Programme)

<table>
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<tr>
<th>Sr. No.</th>
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### Open Elective-2
- (6) Nanomaterials and Nanotechnology
- (7) Green Energy
- (8) Industry 4.0
- (9) Operations Research
- (10) Entrepreneurship Development Program
### Semester IV (M. Tech.- 2 Year Programme)

<table>
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<td>450</td>
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**Abbreviations:** L-No. of Lecture hours per week, T-No. of Tutorial hours per week, P-No. of Practical hours per week, CT-Class Test Marks, TA-Marks of teacher’s assessment including student’s class performance and attendance,

<table>
<thead>
<tr>
<th>1 Hr Lecture</th>
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<th>2 or 3 Hr Practical</th>
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### Course Structure and Scheme of Examination for B.Tech.-M. Tech. Dual 1 Year M.Tech. Programme

#### VLSI Design

**Semester III**

<table>
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<tr>
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<td>CT   TA   Total</td>
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**Semester IV (B.Tech.-M. Tech. Dual 1 Year M.Tech. Programme)**

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**Professional elective -IV**

1. Algorithms for VLSI Design Automation
2. Sensors and Actuators
3. Design for Testability

**Open Elective**

1. IoT and its Applications
2. Artificial Intelligence and Machine Learning
3. Composite Materials
4. Industrial Safety
5. Non-Conventional Energy Sources
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Advanced Mathematics (AHT-301)

L:T:P:  3:1:0  

Course objectives:

From this course, students will be able to:
1. learn distinct methods of solving simultaneous equations.
2. well-versed with partial differential equations and their solutions and applications.
3. acquire the knowledge of transformation to ease the complex problems.
4. acquaintance with basics of random variables and their distribution for dealing with events by chance.
5. study different mathematical domains to deal with real-time engineering problems.

Learning outcomes:

1. Comprehend with engineering problems in different mathematical realm.
2. Learn analytical and numerical methods to deal with mathematical problems.
3. Understand how to model the engineering problems and their solutions.
4. Implement the solutions to real-time complex engineering problems.
5. Apprehend with mathematical methodology.

Course content:

Unit I: Solution of linear simultaneous equations:  
(8 hours)

Consistency, Iterative method, Convergence, Cholesky’s (Crout’s) method, Gauss-Jordan method, Gauss-Seidel iteration and relaxation methods, Solution of Eigenvalue problems, Smallest, largest, and intermediate Eigen values

Computer based algorithm and programme for these methods (non-evaluative)

Unit II: Partial differential equation and its applications:  
(10 hours)
Introduction and classification of partial differential equation, Four standard forms of non-linear partial differential equations and their solutions, linear equations with constant coefficients. Applications of partial differential equations one and two-dimensional wave equation, one and two-dimensional heat equation, Two-dimensional Laplace’s equation.

Unit III: Transform calculus-I: 

Laplace transform, Properties of Laplace transform, Inverse Laplace transform, Applications of Laplace transform, Fourier integral theorem, Fourier transforms, Application of Fourier transform 

Unit IV: Transform calculus-II: 

Z-transform, Properties of Z-transform, Shifting theorems, Initial and final value theorem, Convolution theorems, Inverse Z-transform, Application of Z-transform 

Unit V: Basic probability theory: 

Concept and laws of probability, Discrete and continuous random variable and their distributions; Some special distributions such as Binomial, Poisson, Negative Binomial, Geometric, Continuous uniform, Normal, Exponential, Weibull, Moments, Moment generating functions, Expectation and variance 

Practical demo with statistical software like R, SPSS, SAS, etc. (non-evaluative) 

Text Books / References: 

CMOS Analog Circuit Design (VDT-301)

L:T:P:: 3:1:0

COURSE OBJECTIVES:

From this course, students will be able to:

1. Design and implement the product level opamps and buffers for VLSI applications
2. Study the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs.
3. Understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability

COURSE OUTCOMES (COs):

1: Understanding of advantages and limitations of CMOS analog circuits
2: Appreciation of relative merits and demerits of various MOS current mirrors
3: Develop an understanding of the design considerations of CMOS op-amps and OTAs
4: Capability of analyzing CMOS translinear and square domain circuits
5: Ability to design some CMOS analog circuits employing modern circuit concepts

COURSE CONTENT:

UNIT-1 : Importance, advantages and limitations of CMOS analog circuits; common source amplifier and source follower; differential amplifier; offset voltage determination; Frequency response; noise analysis; voltage follower, Flipped voltage follower (8 hours)
UNIT-2 : IC biasing-current sources, current mirrors and current-steering circuits, Wilson current mirror, Cascode and modified Wilson Current Mirrors; Comparative analysis of various Current mirrors and their features (8 hours)
UNIT-3 :CMOS op-amps: typical architectures, compensation techniques; stability considerations; analysis and design; CMOS OTAs and CMOS single-ended transconductors (8 hours)
UNIT-4: Translinear principle, TL circuits, MOS TL circuits, Square root domain circuits, Typical examples of MOS translinear circuits; Current Conveyors, CFOAs and other modern building blocks (8 hours)
UNIT-5: General Techniques of non-linearity cancellation in MOS analog circuits and their applications; Linearized transconductors, CMOS VCR realisation; CMOS multipliers/dividers; squarers and square-rooters (8 hours)
Text Books:


References:

Digital System Design Using Verilog (VDT-302)

COURSE OBJECTIVES:

From this course, students will be able to:

1. Design and operation of semiconductor memories frequently used in application specific digital system
2. Design and diagnosis of processors and I/O controllers used in embedded systems

COURSE OUTCOMES:

At the end of the course the student will be able to:

1. To understand the concepts of VLSI design flow using HDL.
2. To understand the Design concept of the combinational Circuits.
3. To understand the Design concept of the Sequential Circuits
4. To understand, how to employ EDA tools to model a digital system.
5. To understand, how to Write test benches to verify the design.

UNIT 1: INTRODUCTION TO VLSI AND CAD TOOLS: Evolution of CAD, emergence of HDLs, typical HDL-based design flow, Verilog HDL. Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, simulation and synthesis, system task, test bench, programming language interface, simulation and synthesis tools. (8 hours)

UNIT 2: LANGUAGE CONSTRUCT AND CONVENTION IN VERILOG: Introduction, keywords, identifiers, white space characters, comments, numbers, strings, logic value, strengths, data type, scalars and vectors, parameters, memory, operators.

Gate-Level Modeling: Introduction, module structure, design of flip-flops with gate primitives, delays, net types. (8 hours)

UNIT 3: DATA FLOW LEVEL MODELING: Introduction, Continuous assignments structure, delays and continuous assignments, assignment to vectors, operators. (8 hours)

BEHAVIORAL MODELING: Introduction, operations and assignments, initial construct, always construct, assignment with delay, wait construct, blocking and non-blocking assignment, assign-deassign construct, for loop, while loop, force-release construct, parallel blocks. (8 hours)

UNIT 4: TASKS AND FUNCTIONS DESIGN: Introduction, function, structure and scope of function, task enabling, user defined primitive: combinational and sequential user defined primitive, path delay, system task and functions, file based task and function. (8 hours)
UNIT 5: QUEUES AND FINITE STATE MACHINE: Introduction, task for queue initialization, task for adding and removing from the queue, design of finite state machine: Moore machine and Mealy machine. (8 hours)

BOOKS:
Semiconductor Devices Theory and Modelling (VDT-303)

L:T:P::3:1:0  
Credits-4

COURSE OBJECTIVES:

From this course, students will be able to:

1. Theory of operation, modeling, parameter extraction, scaling issues, and higher order effects of active and passive semiconductor devices
2. Understand the latest models for the devices that are valid out to very high frequencies and the use of physical device modeling.

COURSE OUTCOMES

1. Understand the basic properties of semiconductors including the band gap, charge carrier concentration, doping and charge carrier injection/excitation.
2. Explain the working, design considerations and applications of various semiconducting devices including p-n junctions, BJT and Metal semiconductor Junction.
3. Understand the basics of MOS modelling.
4. Analyse and Model the MOSFET devices
5. Understand the comprehensive idea about small geometry effects.

Course Contents:


(8 hours)


(8 hours)

UNIT-3 MOS Electrostatics in two terminal MOS structure: Energy band diagram in equilibrium and under bias, Flat band voltage, Potential Balance and charge balance, Effect of gate body voltage on surface condition, Accumulation and depletion, Inversion, CV Characteristics, Frequency response. Three terminal MOS Structure: Introduction, Contacting the Inversion layer, the body effect, Regions of inversion, VCB control.  

(8 hours)

UNIT-4 Four terminal MOS Structure: Introduction, Transistor region of operation, Complete all region model, Simplified all region models, Model based on Quasi-Fermi Potential, Regions of
inversion in terms of terminal voltages, strong inversion, weak inversion, moderate inversion, source referenced vs body referenced modelling, effective mobility, temperature effects.


Text Books:
4. Operation and modeling of the MOS transistor by YannisTsividis, Oxford University Press, 2011
Research Methodology and IPR (AHT-302)

L:T:P: 2:0:0

Course Objectives: Students will be able to:
1. To understand the fundamentals of research in today’s world controlled by technology, ideas, concept, and creativity.
2. To understand different methods of research designing and data collections.
3. To understand the methods of report writing and its different methods of interpretations.
4. To understand research ethics and methods of research publications.
5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Course Outcomes:
1. To understand research problem formulation.
2. To study research design and method of data collections.
3. To study methods of report writing.
4. To follow research ethics.
5. To enhance student’s competence to discover new inventions.

Syllabus Contents:

UNIT I: FUNDAMENTAL OF RESEARCH

Meaning of research; objectives of research; basic steps of research; criteria of good research; Research methods vs. Methodology. Types of research – criteria of good research; Meaning of research problem; selection of research problem; Approaches of investigation of solutions for research problem, Errors in selecting a research problem, Scope and objectives of research problem, Review of related literature–Meaning, necessity and sources. (8 hours)

Unit 2: RESEARCH DESIGN AND DATA COLLECTION

Research design: Types of research design- exploratory, descriptive, diagnostic and experimental; Variables- Meaning and types; Hypothesis- Meaning, function and types of hypothesis; Null/Alternative hypothesis; Sampling- Meaning and types of sampling; Probability and Non-Probability; Tools and
techniques of data collection- questionnaire, schedule, interview, observation, case study, survey etc. 

Unit 3: REPORT WRITING AND ITS INTERPRETATION


Unit 4: RESEARCH ETHICS AND SCHOLARY PUBLISHING

Ethics-ethical issues, ethical committees (human & animal); scholarly publishing- IMRAD concept and design of research paper, citation and acknowledgement, plagiarism and its concept and importance for scholar.

Unit 5: INTELLECTUAL PROPERTY RIGHT (IPR)


Reference Books:

2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”
Low Power VLSI Design (VDT 304)

L:T:P::3:0:0

COURSE OBJECTIVES:

From this course, students will be able to:

1. Improvise on the latest techniques used for designing power-efficient logic gates, latches, and flip-flops
2. Learn the latest MOS and bipolar models; breakthroughs in copper metallization, isolation and deep submicron processes; and new approaches to designing logic gates, latches, and flip-flops.

COURSE OUTCOMES (COs):

1. To understand the need for low power VLSI chips and basic analog and digital circuits suitable for low power design
2. To understand Gate-level Logic Simulation architectures and Probabilistic Power Analysis
3. To understand transistor Circuit and gate sizing issues
4. To understand Architecture and System level techniques for Power and Performance Management
5. To study Advanced Techniques for power reduction. To understand challenges involved in low power/voltage analog circuits and study of various techniques available

Course Contents:

UNIT-I Introduction to Needs for Low Power VLSI Chips, Charging and Discharging Capacitance, Short-circuit Current in CMOS Circuit, CMOS Leakage Current, Static Current, Basic Principles of Low Power Design, Low Power Figure of Merits, Gate-level Logic Simulation (8 hours)

UNIT-II Probabilistic Power Analysis of Random Logic Signals, Probability and Frequency, Probabilistic Power Analysis Techniques, Signal Entropy, Transistor and Gate Sizing, Transistor and Gate Sizing, Network Restructuring and Reorganization, Special Latches and Flip-flops, Low Power Digital Cell Library, Adjustable Device Threshold Voltage (8 hours)

UNIT-III Logical Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Precomputation Logic, Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM (8 hours)

UNIT-IV Power and Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits (8 hours)
UNIT-V Challenges involved in low power Analog integrated circuits, issues about low supply voltage, roadmap, Techniques to design and implement low voltage/low power analog circuits like self cascode structure, flipped voltage follower, Bulk driven, FGMOS, QFGMOS etc. 

(8 hours)

Reference Books:
System on Chip Design (VDT 305)

L:T:P::3:0:0 Credits-3

COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand the concepts of System on Chip Design methodology for Logic and Analog Cores
2. Understand the concepts of System on Chip Design Validation.
3. Understand the concepts of SOC Testing.

COURSE OUTCOMES (COs):

1. To analyze the functional and nonfunctional performance of the system early in the design process to support design decisions.
2. To analyze hardware/software tradeoffs, algorithms, and architectures to optimize the system based on requirements and implementation constraints.
3. Describe examples of applications and systems developed using a CO-design approach.
4. To appreciate issues in system-on-a-chip design associated with CO-design, such as intellectual property, reuse, and verification.

COURSE CONTENTS:

Unit-I System-level and SoC design methodologies and tools; (8 hours)

Unit-II HW/SW COdesign: analysis, partitioning, real-time scheduling, hardware acceleration; Virtual platform models, CO-simulation and FPGAs for prototyping of HW/SW systems. (8 hours)

Unit-III Transaction-Level Modeling (TLM) and Electronic System-Level (ESL) languages: System C. (8 hours)

Unit-IV High-Level Synthesis (HLS): allocation, scheduling, binding, resource sharing, pipelining; (8 hours)

Unit-V SoC and IP integration, verification and test. (8 hours)

Text Books/References:
COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand about DSP algorithms.
2. Explain about retiming techniques, folding and register minimization path problem.
3. Introduce abut algorithm strength reduction techniques & parallel processing of FIR and IIR filters.
4. Explain about finite word length effects and round off noise computation in DSP

Course Outcomes:

1. Ability to determine the parameters influencing the efficiency of DSP architectures and apply pipelining and parallel processing techniques to alter FIR structures for efficiency
2. Ability to analyze and modify the design equations leading to efficient DSP architectures for transforms apply low power techniques for low power dissipation
3. Ability to speed up convolution process and develop fast and area efficient IIR structures
4. Ability to develop fast and area efficient multiplier architectures
5. Ability to reduce multiplications and build fast hardware for synchronous digital systems

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS: Introduction to DSP systems – typical DSP algorithms, data flow and dependence graphs – critical path, loop bound, iteration bound, longest path matrix algorithm, pipelining and parallel processing of FIR filters, pipelining and parallel processing for low power. (8 hours)

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION: Retiming – definitions and properties, unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even, Merge-Sort architecture, parallel rank-order filters. (8 hours)

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS: Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – advanced techniques – special techniques, adiabatic techniques – physical design, floor planning, placement and routing. (8 hours)

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES: Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save
multipliers, design of lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters (8 hours)

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS WAVE AND ASYNCHRONOUS PIPELINING: Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered singlephase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining - Bundled Dataversus Dual-Rail protocol (8 hours)

REFERENCES
Mixed Signal IC Design (VDT 307)

L:T:P::3:0:0

COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand the mixed signal circuits like DAC, ADC, PLL etc.
2. Gain knowledge on filter design in mixed signal mode.
3. Acquire knowledge on design different architectures in mixed signal mode

COURSE OUTCOMES (COs):

1. To design and perform analysis of fundamental building blocks and basic analog circuits.
2. To introduce circuit design concepts for basic building blocks used in mixed-signal integrated circuit designs.
3. To provide a foundation for more complicated and advanced circuit designs.
4. To handle both practical design and layout issues involved.

COURSE CONTENT:

Unit-I
Analog and discrete-time signal processing, analog integrated continuous-time and discrete-time filters, Analog continuous-time filters, passive and active filters, basics of analog discrete-time filters and Z-transform (8 hours)

Unit-II
Switched-capacitor filters, Non-idealities in switched-capacitor filters, switched capacitor filter architectures, switched capacitor filter applications, (8 hours)

Unit-III
Basics of data converters, Successive approximation ADCs, Dual slope ADCs, Flash ADC, Pipeline ADC (8 hours)

Unit-IV
Hybrid ADC structures, higher solution ADC, DAC, Mixed signal layout, Interconnects and data transmission, Voltage-mode signaling and data transmission, Current-mode signaling and data transmission. (8 hours)

Unit-V
Introduction to frequency synthesizers and synchronization, basics of PLL, Analog PLL, Digital PLL, Delay Locked Loop (DLL). (8 hours)
Text Books/References:

Memory Technologies (VDT-308)

L:T:P::3:0:0

Credits-3

COURSE OBJECTIVES:

From this course, students will be able to:

1. Acquire knowledge about different types of semiconductor memories.
2. Study about architecture and operations of different semiconductor memories.
3. Comprehend the low power design techniques and methodologies.

COURSE OUTCOMES (COs):

1. Analysis the different types of RAM, ROM designs.
2. Analysis the different RAM and ROM architecture and interconnects.
3. Analysis about design and characterization technique.
4. Analysis of different memory testing and design for testability.
5. Identification of new developments in semiconductor memory design.

Course Content:

UNIT 1
Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOI, Advanced SRAM Architectures, Application Specific SRAMs; DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM. (8 hours)

UNIT 2
Non-Volatile Memories: High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. (8 hours)

UNIT 3

UNIT 4
UNIT 5
Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.

(8 hours)

Reference Books:
HARDWARE SOFTWARE CO-DESIGN FOR FPGA (VDT-309 )

L:T:P::3:0:0 Credits-3

COURSE OBJECTIVES:

From this course, students will be able to:

1. Analyzing the control-flow and data-flow of a software program and a cycle-based hardware description
2. Partitioning simple software programs into hardware and software components, and creating appropriate hardware-software interfaces to reflect this partitioning
3. Identifying performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software component

Course Outcomes:

1. Describe The Broad Range of System Architectures and Design Methodologies that currently exist and define their fundamental attributes.
2. Discuss the Dataflow Models as a State-of-the-Art Methodology to Solve Co-Design Problems and to Optimize the balance between Software and Hardware.
5. Understand the Concurrent Specification from an Algorithm, Analyze its behavior and partition the Specification into Software (C Code) and Hardware (HDL) Components

Course Content:


UNIT II HARDWARE/SOFTWARE PARTITIONING: The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of The Partitioning Graph, Formulation of The
HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms. (8 hours)

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS: The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis. (8 hours)


REFERENCE BOOKS:
FPGA System Design (VDT-310)

L:T:P::3:1:0

Credits-4

COURSE OBJECTIVES:

From this course, students will be able to:

1. Learn and use design flow for using FPGA.
2. Learn programming of FPGA with practical circuits
3. Design for higher performance or lower area using alternative circuit families.

Course Outcomes:

1. Describe the architecture of FPGAs and logic design process and implement different logic circuits on the internal architecture of FPGA
2. Write HDL codes of combinational and sequential Circuits and perform their functional verification
3. Design the control unit of a Digital Circuit and implement it using Finite State Machines (FSMs).
4. Design of efficient and high speed adders and multipliers for optimizing the datapath of digital circuits.
5. Analyze Digital design in terms of area, power and speed.

Course Contents:

UNIT-I Introduction: Different kinds of programmable logic devices: Field Programmable Gate Array (FPGA), Programmable Logic Device (PLD), FPGA manufacturers (Xilinx, Altera, Actel, Lattice Semiconductor, Atmel). FPGA applications. Adjoining devices. Instruments and software. (8 hours)

UNIT-II The Structure of FPGA: FPGA general description. Different kinds of FPGA packages. FPGA architecture. Internal hard modules of FPGA (CLB, Block RAM, DCM), their meanings and usage. Different kinds of I/O modules, their usage and configuration. FPGAs Field
Programmable Gate Arrays—Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs. (8 hours)

**UNIT-III** FPGA Design Flow: Architecture design. Project design using Verilog Hardware Description Language (HDL). Defining testing methodology and test bench design. RTL simulation, synthesizing, implementation, gate level simulation of design. Reusing of internal hard modules during design and implementation. (8 hours)

**UNIT-IV** Testing Methodology: Functional and gate level testing. SDF file description and usage. (8 hours)

**UNIT-V** FPGA Configuration: Different types of FPGA configuration files. Generation of configuration file and its loading into FPGA. (8 hours)

**Reference Books:**
VEER MADHO SINGH BHANDARI UTTARAKHAND TECHNICAL UNIVERSITY, DEHRADUN

VLSI CIRCUIT DESIGN (VDT-311)

L:T:P::3:1:0                          Credits-4

COURSE OBJECTIVES:

From this course, students will be able to:

1. Learn digital CMOS logic design.
2. Realize importance of testability in logic circuit design.
3. Overview SoC issues and understand PLD architectures with advanced features.

COURSE OUTCOMES:

At the end of the course the student will be able to:

1. To get acquainted with basic theory of MOS transistors and familiar with CMOS fabrication technology
2. To understand the concepts related to implementation of Combinational CMOS logic circuits
3. To understand the concepts related to implementation of sequential CMOS logic circuits
4. To understand the concepts of memories design with efficient architectures to improve access times, power consumption.
5. To understand the process behind testing of CMOS integrated circuits

UNIT 1: REVIEW OF MOSFET OPERATION AND CMOS PROCESS FLOW:
MOS Threshold voltage, MOSFET I-V characteristics: Long and short channel, MOSFET capacitances, lumped and distributed RC model for interconnects, SPICE Model, CMOS process flow, Layout and design rules. (8 hours)

UNIT 2: CMOS INVERTER AND COMBINATIONAL LOGIC:
The CMOS Inverter, CMOS Logic Gates: NAND Gate, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers, adders, Complex logic circuit. (8 hours)

UNIT 3: SEQUENTIAL LOGIC:
Behaviour of Bistable element, monostable and a stable circuits, Static latches and flip-flops (FFs), dynamic latches and FFs, Voltage Bootstrapping, Synchronous dynamic high Performance dynamic CMOS circuits. (8 hours)

UNIT 4: MEMORIES AND ARRAY STRUCTURES:
MOS-ROM, SRAM cell, memory peripheral circuits, signal to noise ratio, power dissipation. (8 hours)

UNIT 5: TESTING, DEBUGGING, AND VERIFICATION:
Test vectors, Fault Models, Observability, Controllability, Repeatability, Survivability, Fault Coverage, Automatic Test Pattern Generation (ATPG), Delay Fault Testing, Ad Hoc Testing, Scan Design, Built-In Self-Test (BIST), IDDQ Testing, Design for Manufacturability, Boundary Scan etc. (8 hours)
BOOKS:
4. Weste and Harris, “CMOS VLSI Design”
Embedded System Design (VDT-312)

L:T:P::3:1:0 Credits-4

COURSE OBJECTIVES:

From this course, students will be able to:

1. Acquire knowledge about the basic functions, structure, concepts and applications of embedded systems
2. Learn the method of designing and program an Embedded Systems for real time applications
3. Acquire knowledge about the development of embedded software using RTOS and implement small programs to solve well-defined problems on an embedded platform.

COURSE OUTCOMES (COs):

CO1: To develop basic understanding of embedded systems in general and their applications.
CO2: To comprehend the architecture and components of embedded systems.
CO3: To understand the onboard and external communication interfaces.
CO4: To understand the concepts of multiprocessing, multitasking and shared memory.

COURSE CONTENTS:

Unit I
Formal definition of an Embedded System. Embedded system examples. Compare and contrast embedded system and conventional/generic computer system. Overview of elements of an Embedded system. Processor level implementation using (a) generic devices (b) full custom ASIP and (c) Soft core implementation on FPGA. Key parameters of Embedded System Design (Time to market and cost). (8 hours)

Unit II
Microcontroller Classification based on memory access, ISA, data bus width. Example microcontroller families (8-bit, 16-bit and 32-bit examples). Memory technologies, Memory interface busses. Desirable microcontroller features. Development, debugging and testing tools. Elements of Microcontroller ecosystem: Reset, Clock, Power supply and program download options. (8 hours)

Unit III
AVR Microcontroller architecture details. Elements of physical interfacing: Input devices, Output, environmental sensors, actuators. Elements of analog signal processing. Inter and Intra-device communication Interfaces. Real Time Clock. Storage devices. Power supply topologies for embedded systems. (8 hours)

Unit IV
Elements of Embedded C programming; pointers and memory optimization, bit-wise operations, using and creating device library, Compiler optimization. Interrupt driven programming and Foreground-background programming model. (8 hours)

Unit V

Text Books:

Testing of VLSI Circuits (VDT-313)

L:T:P:: 3:1:0
Credits-4

COURSE OBJECTIVES:

From this course, students will be able to:

Deal with the study of VLSI design flow, Functional verification, verification flow, need of electronic testing, fault modeling, test generation for combinational circuits

COURSE OUTCOMES (COs):

1. Study of test generation for sequential circuits, fault simulation.
2. Study of Built-In Self-Test (BIST), Memory testing, Design for Testability (DFT)
3. Study of SoC test, fault diagnosis, Analog/RF tests.

Course Contents:

UNIT I - BASICS OF TESTING AND FAULT MODELING (8 hours)

Introduction- Principle of testing - types of testing - DC and AC parametric tests - fault modeling- Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation

UNIT II - TESTING AND TESTABILITY OF COMBINATIONAL CIRCUITS (8 hours)


UNIT III - TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS (8 hours)

Testing of sequential circuits as iterative combinational circuits - state table verification - test generation based on circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) - partial scan - Boundary scan

UNIT IV - MEMORY, DELAY FAULT AND IDDQ TESTING (8 hours)

Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults –Delay test- IDDQ testing - testing methods - limitations of IDDQ Testing

UNIT V - BUILT-IN SELF-TEST (8 hours)
Test pattern generation of Built-in Self-Test (BIST) - Output response analysis – BIST architectures.

**Reference Books:**
ASIC DESIGN USING VERILOG (VDT-314)

L:T:P:: 3:1:0

Credits-4

COURSE OBJECTIVES:
From this course, students will be able to:

1. Understand how modern digital systems are designed based around the use of hardware description languages, logic synthesis and mapping onto standard cell and field programmable logic.
2. Understand non-logic-design issues in ASIC design, including timing, power, and verification.
3. Know how to approach block level optimization in ASIC design.

COURSE OUTCOMES:
At the end of the course, the student will be able to:

1. Explain VLSI design flow using HDL.
2. Design the combinational and sequential digital systems.
3. Employ EDA tools to model a digital system.
4. Write test benches to verify the design.

Course Contents:

UNIT 1: INTRODUCTION TO VLSI AND CAD TOOLS: Evolution of CAD, emergence of HDLs, typical HDL-based design flow, Verilog HDL. Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, simulation and synthesis, system task, test bench, programming language interface, simulation and synthesis tools. (8 hours)

UNIT 2: LANGUAGE CONSTRUCT AND CONVENTION IN VERILOG: Introduction, keywords, identifiers, white space characters, comments, numbers, strings, logic value, strengths, data type, scalars and vectors, parameters, memory, operators.
Gate-Level Modeling: Introduction, module structure, design of flip-flops with gate primitives, delays, net types. (8 hours)

UNIT 3: DATAFLOW LEVEL MODELING: Introduction, Continuous assignments structure, delays and continuous assignments, assignment to vectors, operators.
BEHAVIORAL MODELING: Introduction, operations and assignments, initial construct, always construct, assignment with delay, wait construct, blocking and non-blocking assignment, assign-deassign construct, for loop, while loop, force-release construct, parallel blocks. (8 hours)
UNIT 4: TASKS AND FUNCTIONS DESIGN: Introduction, function, structure and scope of function, task enabling, user defined primitive: combinational and sequential user defined primitive, path delay, system task and functions, file based task and function. (8 hours)

UNIT 5: QUEUES AND FINITE STATE MACHINE: Introduction, task for queue initialization, task for adding and removing from the queue, design of finite state machine: Moore machine and Mealy machine. (8 hours)

BOOKS:
Algorithms for VLSI Design Automation (VDT-315)

L:T:P:: 3:0:0

COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand techniques for electronic design automation (EDA), a.k.a. computer-aided design (CAD)
2. Study IC technology evolution and their impacts on the development of EDA tools

COURSE OUTCOMES:

1. Understand the basic concept of VLSI.
2. Differentiate analog and digital VLSI design cycle.
3. Apply appropriate automation algorithms for partitioning, floor planning, placement and routing.
4. Design clock trees to distribute the clock signals on the chip while satisfying various constraints like clock skew and wire length.

Course Contents:

UNIT 1: VLSI physical design automation and Fabrication: VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices (8 hours)

UNIT 2: VLSI automation Algorithms Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing. (8 hours)

UNIT 3: Floor planning & pin assignment: Problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block& cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment Placement Problem formulation, classification of placement algorithms, simulation base placement algorithms, recent trends in placement (8 hours)

UNIT 4: Global Routing and Detailed routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms. (8 hours)
UNIT 5: Over the cell routing & via minimization: Two layers over the cell routers, constrained & unconstrained via minimization Compaction: Problem formulation, classification of compaction algorithms, One dimensional compaction, two dimension based compaction, hierarchical compaction. (8 hours)

Reference Books:
COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand the operation of commonly employed sensors and actuators
2. Be able to analyze and select the most appropriate sensors or actuator for an application.
3. Be able to design and construct the appropriate interface circuits for the sensors and actuators.

COURSE OUTCOMES (COs):

1. Interpret physical principles applied in sensors and actuators
2. To model and design sensors with desired physical and chemical properties
3. Identify various types of sensors including thermal, mechanical, electrical, electromechanical and optical sensors
4. To implement sensors for physical, chemical, and biochemical applications

Course Contents:


(8 hours)


(8 hours)


(8 hours)

(8 hours)


(8 hours)

Reference Books:
COURSE OBJECTIVES:

From this course, students will be able to:

1. Apply the concepts in testing which can help them design a better yield in IC design
2. Tackle the problems associated with testing of semiconductor circuits at earlier design levels
3. Identify the design for testability methods for combinational & sequential CMOS circuits

COURSE OUTCOMES (COs):

CO1: To understand types of faults and also to study about fault detection
CO2: To understand the concepts of the test generation methods.
CO3: To understand the fault diagnosis methods will learn testing and verification in VLSI design process
CO4: To understand Automatic test pattern generation concepts for combinational and sequential circuits
CO 5: To perform memory test, defect screening, SOC testing etc

COURSE CONTENTs:

Unit-I

Unit-II

Unit-III
Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan. (8 hours)

Unit-IV
Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.
Unit-V
Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions. (8 hours)

Text Books/References:
Technical Writing and Presentation Skills (AHT-303)

L:T:P::2:0:0 Non-credits

Course Objectives:
- To develop effective writing and presentation skills in students.
- To develop textual, linguistic and presentation competencies in students appropriate for their professional careers.

Course Outcomes:
After the successful completion of course, the students will be able to:
CO1: Write clearly and fluently to produce effective technical documents.
CO2: Demonstrate an appropriate communication style to different types of audiences both orally and written as per demand of their professional careers.
CO3: Communicate in an ethically responsible manner.

Course Contents:

WRITING SKILLS

Unit-I
Technical Writing-Basic Principles: Words-Phrases-Sentences, Construction of Cohesive Paragraphs, Elements of Style.

Unit-II
Principles of Summarizing: Abstract, Summary, Synopsis

Unit-III
Technical Reports: Salient Features, Types of Reports, Structure of Reports, Data Collection, Use of Graphic Aids, Drafting and Writing

PRESENTATION SKILLS

Unit-IV

Unit-V

References: