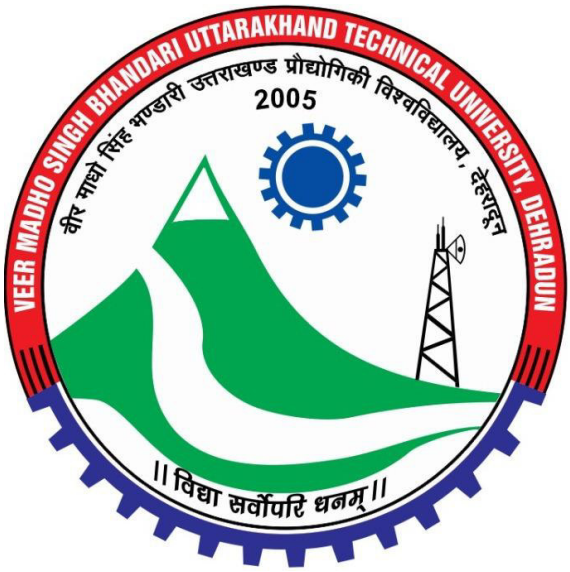
VEER MADHO SINGH BHANDARI UTTARAKHAND TECHNICAL UNIVERSITY

(Formerly Uttarakhand Technical University, Dehradun Established by Uttarakhand State Govt. wide Act no. 415 of 2005)
Suddhowala, PO-Chandanwadi, Premnagar, Dehradun, Uttarakhand (Website- www.uktech.ac.in)



SYLLABUS

For

Master of Engineering Programmes

(M.Tech. VLSI DESIGN)

(For admission in 2022-23 and onwards)

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Courses Structure and Scheme of Examination for M. Tech.- 2 Year Programme VLSI Design

Semester I											
Sr. No.	**Course Type/Code**	**Course Name**	**Teaching Scheme**			**Credits**	**Internal Marks**			**External Marks**	**Total Marks**
			L	**T**	**P**		**CT**	**TA**	**Total**		
1	VDT301	CMOS Analog Circuit Design	3	1	0	4	30	20	50	100	150
2	VDT302	Digital System Design Using Verilog	3	1	0	4	30	20	50	100	150
3	VDT303	Semiconductor Devices Theory and Modelling	3	1	0	4	30	20	50	100	150
4	VDT30X	Professional Elective-I	3	0	0	3	30	20	50	100	150
5	VDT30X	Professional Elective-II	3	0	0	3	30	20	50	100	150
6	VDP301	CMOS Analog Circuit Design using Spice	0	0	3	1		25	25	25	50
7	VDP302	Digital System Design Using Verilog lab	0	0	3	1		25	25	25	50
8	AHT-302	Research Methodology and IPR	2	0	0	2		50	50	50	100
9	AHT-303	Technical Writing and Presentation Skill	2	0	0	NC		50	50	0	NC
		Total	**22**	**3**	**8**	**22**	**150**	**250**	**400**	**600**	**950**
10	OET30X	Open Elective (Optional)	3	0	0	3	30	20	50	100	150

Professional Elective-I	**Professional elective -II**
(4) Low Power VLSIDesign (5) **System** on Chip Design (6) VLSI Signal Processing	(7) Mixed Signal IC Design (8) Memory Technologies (9) Hardware and Software Co-Design
Open Elective(Optional)	
(1) IoT and its Applications (2) Artificial Intelligence and Machine Learning (3) Composite Materials	(4) Industrial Safety (5) Non-Conventional Energy Sources

Semester II (M. Tech.- 2 Year Programme)											
Sr. No.	**Course Type/Code**	**Course Name**	**Teaching Scheme**			**Credits**	**Internal Marks**			**External Marks**	**Total Marks**
			L	**T**	**P**		**CT**	**TA**	**Total**		
1	VDT310	FPGA Based System Design	3	1	0	4	30	20	50	100	150
2	VDT311	VLSI Circuit Design	3	1	0	4	30	20	50	100	150

3	VDT31X	Professional Elective-III	3	1	0	4	30	20	50	100	150
4	VDT31X	Professional Elective-IV	3	0	0	3	30	20	50	100	150
5	OET30X	Open Elective-2	3	0	0	3	30	20	50	100	150
6	VDP303	Lab-III:VLSI Design Lab	0	0	3	1		25	25	25	50
7	VDP304	Lab- IV: TCAD Lab	0	0	3	1		25	25	25	50
		Total	**15**	**3**	**6**	**20**			**300**	**550**	**850**
8	OET30X	Open Elective-2 (Optional)	3	0	0	3	30	20	50	100	150

Professional Elective-III	**Professional elective -IV**
(2) Embedded System Design (3) Testing of VLSI Circuits (4) ASIC Design ESIGN Using Verilog	(5) Algorithms for VLSI Design Automation (6) Sensors and Actuators (7) Design for Testability
Open Elective-2	
(1) IoT and its Applications (2) Artificial Intelligence and Machine Learning (3) Composite Materials	(4) Industrial Safety (5) Non-Conventional Energy Sources

Semester III(M. Tech.- 2 Year Programme)											
Sr. No.	**Course Type/Code**	**Course Name**	**Teaching Scheme**			**Credits**	**Internal Marks**			**External Marks**	**Total Marks**
			L	T	P		**CT**	**TA**	**Total**		
1	OET30X	Open Elective-2	3	0	0	3	30	20	50	100	150
2	VDP305	Seminar	0	0	4	2		100	100		100
3	VDP306	Project	0	0	10	5		100	100	150	250
4	VDP307	Dissertation	0	0	12	6		300	300		300
		Total	**3**	**0**	**22**	**16**		**520**	**550**	**250**	**800**

Open Elective-2
(6) Nanomaterials and Nanotechnology
(7) Green Energy
(8) Industry4.0
(9) Operations Research
(10) Entrepreneurship Development Program

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Semester IV(M. Tech.- 2 Year Programme)											
Sr. No.	**Course Type/Code**	**Course Name**	**Teaching Scheme**			**Credits**	**Internal Marks**			**External Marks**	**Total Marks**
			L	T	P		**CT**	**TA**	**Total**		
1	VDP308	Dissertation	0	0	28	14		250	250	450	700
		Total	**0**	**0**	**28**	**14**		**250**	**250**	**450**	**700**

Abbreviations: L-No. of Lecture hours per week, T-No. of Tutorial hours per week, P-No. of Practical hours per week, CT-Class Test Marks, TA-Marks of teacher's assessment including student's class performance and attendance,

1 Hr Lecture	**1 Hr Tutorial**	**2 or 3 Hr Practical**
1 Credit	**1 Credit**	**1 Credit**

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Course Structure and Scheme of Examination for B.Tech.-M. Tech. Dual 1 Year M.Tech. Programme VLSI Design

Semester III											
Sr. No.	**Course Type/Code**	**Course Name**	**Teaching Scheme**			**Credits**	**Internal Marks**			**External Marks**	**Total Marks**
			L	T	P		**CT**	**TA**	**Total**		
1	AHT-301	Advanced Mathematics	3	1	0	4	30	20	50	100	150
2	VDT310	FPGA Based System Design	3	1	0	4	30	20	50	100	150
3	OET30X	Open Elective	3	0	0	3	30	20	50	100	150
4	AHT-302	Research Methodology and IPR	2	0	0	2	30	20	50	50	100
5	VDP305	Seminar	0	0	4	2		100	100		100
6	VDP306	Project	0	0	10	5		100	100	150	250
7	VDP307	Dissertation	0	0	12	6		300	300		300
		Total	**11**	**2**	**26**	**26**	**120**	**580**	**700**	**500**	**1200**

Semester IV (B.Tech.-M. Tech. Dual 1 Year M.Tech. Programme)											
Sr. No.	**Course Type/Code**	**Course Name**	**Teaching Scheme**			**Credits**	**Internal Marks**			**External Marks**	**Total Marks**
			L	T	P		**CT**	**TA**	**Total**		
1		Advance VLSI Technology	3	1	0	4	30	20	50	100	150
2	VDT31X	Professional Elective I/II/IV	3	0	0	3	30	20	50	100	150
3	OET30X	Open Elective	3	0	0	3	30	20	50	100	150
4		Lab-I	0	0	3	1		25	25	25	50
5		Lab-II	0	0	3	1		25	25	25	50
6	VDP308	Dissertation	0	0	28	14		250	250	450	700
		Total	**9**	**1**	**34**	**26**	**90**	**360**	**450**	**800**	**1250**

Professional elective -IV	**Open Elective**
(4) Algorithms for VLSI Design Automation (5) Sensors and Actuators (6) Design for Testability	(1) IoT and its Applications (2) Artificial Intelligence and Machine Learning (3) Composite Materials (4) Industrial Safety (5)Non-Conventional Energy Sources

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Abbreviations:L-No. of Lecture hours per week, T-No. of Tutorial hours per week, P-No. of Practical hours per week, CT-Class Test Marks, TA-Marks of teacher's assessment including student's class performance and attendance,

1 Hr Lecture	1 Hr Tutorial	2 or 3 Hr Practical
1 Credit	1 Credit	1 Credit

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Advanced Mathematics (AHT-301)

L:T:P:: 3:1:0 **Credits-4**

Course objectives:

From this course, students will be able to:

1. learn distinct methods of solving simultaneous equations.
2. well-versed with partial differential equations and their solutions and applications.
3. acquire the knowledge of transformation to ease the complex problems.
4. acquaintance with basics of random variables and their distribution for dealing with events by chance.
5. study different mathematical domains to deal with real-time engineering problems.

Learning outcomes:

1. Comprehend with engineering problems in different mathematical realm.
2. Learn analytical and numerical methods to deal with mathematical problems.
3. Understand how to model the engineering problems and their solutions.
4. Implement the solutions to real-time complex engineering problems.
5. Apprehend with mathematical methodology.

Course content:

Unit I: Solution of linear simultaneous equations: (8 hours)

Consistency, Iterative method, Convergence, Cholesky's (Crout's) method, Gauss-Jordan method, Gauss-Seidel iteration and relaxation methods, Solution of Eigenvalue problems, Smallest, largest, and intermediate Eigen values

Computer based algorithm and programme for these methods (non-evaluative)

Unit II: Partial differential equation and its applications: (10 hours)

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Introduction and classification of partial differential equation, Four standard forms of non-linear partial differential equations and their solutions, linear equations with constant coefficients. Applications of partial differential equationsone and two-dimensional wave equation, one and two-dimensional heat equation, Two-dimensional Laplace's equation.

Unit III: Transform calculus-I: (8 hours)

Laplace transform, Properties of Laplace transform, Inverse Laplace transform,Applications of Laplace transform, Fourier integral theorem, Fourier transforms, Application of Fourier transform

Unit IV: Transform calculus-II: (8 hours)

Z-transform, Properties of Z-transform, Shifting theorems, Initial and final value theorem, Convolution theorems, Inverse Z-transform, Application of Z-transform

Unit V: Basic probability theory: (8 hours)

Concept and laws of probability, Discrete and continuous random variable and their distributions; Some special distributions such as Binomial, Poisson, Negative Binomial, Geometric, Continuous uniform, Normal, Exponential, Weibull, Moments,Moment generating functions, Expectation and variance

Practical demo with statistical software like R, SPSS, SAS, etc. (non-evaluative)

Text Books / References:

1. B.S. Grewal, Engineering Mathematics, Khanna Publications, 44th edition.
2. F.B. Hilderbrand, Method of Applied Mathematics, PHI Publications, 2nd edition.
3. M.D. Raisinghania, Ordinary and Partial Differential Equations, S. Chand Publication, 20th edition.
4. S.C. Gupta and V.K. Kapoor, Fundamentals of Mathmematical Statistics, S. Chand Publication, 4th edition.
5. Erwin Kreyszig, Advanced Engineering Mathematics, John Wiley & Sons, 10th edition.
6. S. Ross, A First Course in Probability, Pearson Education, 8th edition.

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CMOS Analog Circuit Design (VDT-301)

L:T:P:: 3:1:0 **Credits-4**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Design and implement the product level opamps and buffers for VLSI applications
2. Study the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs.
3. Understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability

COURSE OUTCOMES (COs):

1: Understanding of advantages and limitations of CMOS analog circuits

2: Appreciation of relative merits and demerits of various MOS current mirrors

2: Develop an understanding of the design considerations of CMOS op-amps and OTAs

4: Capability of analyzing CMOS translinear and square domain circuits

5: Ability to design some CMOS analog circuits employing modern circuit concepts

COURSE CONTENT:

UNIT-1 : Importance, advantages and limitations of CMOS analog circuits; common source amplifier and source follower; differential amplifier; offset voltage determination; Frequency response; noise analysis; voltage follower, Flipped voltage follower **(8 hours)**

UNIT-2 : IC biasing-current sources, current mirrors and current-steering circuits, Wilson current mirror, Cascode and modified Wilson Current Mirrors; Comparative analysis of various Current mirrors and their features **(8 hours)**

UNIT-3 :CMOS op-amps: typical architectures, compensation techniques; stability considerations; analysis and design; CMOS OTAs and CMOS single-ended transconductors **(8 hours)**

UNIT-4: Translinear principle, TL circuits, MOS TL circuits, Square root domain circuits, Typical examples of MOS translinear circuits; Current Conveyors, CFOAs and other modern building blocks **(8 hours)**

UNIT-5: General Techniques of non-linearity cancellation in MOS analog circuits and their applications; Linearized transconductors, CMOS VCR realisation; CMOS multipliers/dividers; squarers and square-rooters. **(8 hours)**

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Text Books:

1. Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press.

2. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata-McGraw Hill.

References:

1. Gray R., Paul, Hurst, J. Paul, Lewis H. Stephen and Meyer G. Robert, Analysis and Design of Analog Integrated Circuits, John Wiley and Sons.

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Digital System Design Using Verilog (VDT-302)

L:T:P::3:1:0 **Credits-4**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Design and operation of semiconductor memories frequently used in application specific digital system
2. Design and diagnosis of processors and I/O controllers used in embedded systems

COURSE OUTCOMES:

At the end of the course the student will be able to:

1. To understand the concepts of VLSI design flow using HDL.
2. To understand the Design concept of the combinational Circuits.
3. To understand the Design concept of the Sequential Circuits
4. To understand, how to employ EDA tools to model a digital system.
5. To understand, how to Write test benches to verify the design.

UNIT 1: INTRODUCTION TO VLSI AND CAD TOOLS: Evolution of CAD, emergence of HDLs, typical HDL-based design flow, Verilog HDL. Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, simulation and synthesis, system task, test bench, programming language interface, simulation and synthesis tools. **(8 hours)**

UNIT 2: LANGUAGE CONSTRUCT AND CONVENTION IN VERILOG: Introduction, keywords, identifiers, white space characters, comments, numbers, strings, logic value, strengths, data type, scalars and vectors, parameters, memory, operators.

Gate-Level Modeling: Introduction, module structure, design of flip-flops with gate primitives, delays, net types. **(8 hours)**

UNIT 3: DATA FLOW LEVEL MODELING: Introduction, Continuous assignments structure, delays and continuous assignments, assignment to vectors, operators. **(8 hours)**

BEHAVIORAL MODELING: Introduction, operations and assignments, initial construct, always construct, assignment with delay, wait construct, blocking and non-blocking assignment, assign-deassign construct, for loop, while loop, force-release construct, parallel blocks.

(8 hours)

UNIT 4: TASKS AND FUNCTIONS DESIGN: Introduction, function, structure and scope of function, task enabling, user defined primitive: combinational and sequential user defined primitive, path delay, system task and functions, file based task and function. **(8 hours)**

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UNIT 5: QUEUES AND FINITE STATE MACHINE: Introduction, task for queue initialization, task for adding and removing from the queue, design of finite state machine: Moore machine and Mealy machine. **(8 hours)**

BOOKS:

1. Samir Palnitkar, "Verilog HDL, A Guide to Digital Design and Synthesis", Second Edition, Pearson Education, 2004
2. T.R. Padmanabhan, B. Bala Tripura Sundari "Design through Verilog HDL" Wiley India Pvt. Ltd, 2008
3. J. Bhaskar, "Verilog HDL Synthesis", BS publications, 2001.

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Semiconductor Devices Theory and Modelling (VDT-303)

L:T:P::3:1:0 **Credits-4**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Theory of operation, modeling, parameter extraction, scaling issues, and higher order effects of active and passive semiconductor devices
2. Understand the latest models for the devices that are valid out to very high frequencies and the use of physical device modeling.

COURSE OUTCOMES

1. Understand the basic properties of semiconductors including the band gap, charge carrier concentration, doping and charge carrier injection/excitation.
2. Explain the working, design considerations and applications of various semiconducting devices including p-n junctions, BJT and Metal semiconductor Junction.
3. Understand the basics of MOS modelling.
4. Analyse and Model the MOSFET devices
5. Understand the comprehensive idea about small geometry effects.

Couse Contents:

UNIT-1 Band structure: Band structure evolution, E- k relation, Density of states, Carrier Statistics, Semiconductors in Equilibrium and Carrier Transport in Semiconductors: Semiconductor Materials, Carrier Concentration, Carrier Drift, Carrier Diffusion, Generation and Recombination Process, Continuity Equation, Thermionic Emission, Tunnelling, Ballistic Transport, High Field Effects. **(8 hours)**

UNIT-2 Physics of Junction Devices: Thermal Equilibrium Condition, Depletion Region, Depletion and Diffusion Capacitances, Current-Voltage Characteristics, Charge Storage and Transient Behaviour, Junction Breakdown, Metal Semiconductor Contacts. Physics of Bipolar devices: Transistor Action, Static Characteristics, Frequency Response and Switching, Hetero junction. **(8 hours)**

UNIT-3 MOS Electrostatics in two terminal MOS structure: Energy band diagram in equilibrium and under bias, Flat band voltage, Potential Balance and charge balance, Effect of gate body voltage on surface condition, Accumulation and depletion, Inversion, CV Characteristics, Frequency response.Three terminal MOS Structure: Introduction, Contacting the Inversion layer, the body effect, Regions of inversion, VCB control. **(8 hours)**

UNIT-4 Four terminal MOS Structure: Introduction, Transistor region of operation, Complete all region model, Simplified all region models, Model based on Quasi-Fermi Potential, Regions of

inversion in term of terminal voltages, strong inversion, weak inversion, moderate inversion, source referenced vs body referenced modelling, effective mobility, temperature effects.

(8 hours)

UNIT-5 Small Dimension Effects: Introduction, carrier velocity saturation, channel length modulation, charge sharing, drain induced barrier lowering, punch through, hot carrier effects, poly silicon depletion, quantum mechanical effects, DC gate current, junction leakage: band to band tunnelling and GIDL, leakage currents. Ballistic FET: Introduction, channel transmission, Introduction to the Virtual source model. **(8 hours)**

Text Books:

1. Semiconductor Device Fundamentals by Robert F. Pierret ,Pearson; 1st edition (1 January 2006)
2. Semiconductor Devices: Modeling and Technology by A Dasgupta, N. Dasgupta, Prentice hall India Private Limited, 2004.
3. Semiconductor Devices, Physics and Technology, 3ed by S. M. Sze, Wiley; Eighth edition (1 January 2015)..
4. Operation and modeling of the MOS transistor by YannisTsividis, Oxford University Press, 2011

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Research Methodology and IPR (AHT-302)

L:T:P:: 2:0:0 **Credits-2**

Course Objectives: Students will be able to:

1. To understand the fundaments of research in today's world controlled by technology, ideas, concept, and creativity.
2. To understand different methods of research designing and data collections.
3. To understand the methods of report writing and its different methods of interpretations.
4. To understand research ethics and methods of research publications
5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and inturn brings about, economic growth and social benefits.

Course Outcomes:

1. To understand research problem formulation.
2. To study research design and method of data collections.
3. To study methods of report writing.
4. To follow research ethics.
5. To enhance student's competence to discover new inventions.

Syllabus Contents:

UNIT I: FUNDAMENTAL OF RESEARCH

Meaning of research; objectives of research; basic steps of research; criteria of good research; Research methods vs. Methodology. Types of research –criteria of good research; Meaning of research problem; selection of research problem; Approaches of investigation of solutions for research problem, Errors in selecting a research problem, Scope and objectives of research problem, Review of related literature-Meaning, necessity and sources. **(8 hours)**

Unit 2: RESEARCH DESIGN AND DATA COLLECTION

Research design: Types of research design- exploratory, descriptive, diagnostic and experimental; Variables- Meaning and types; Hypothesis- Meaning, function and types of hypothesis; Null/Alternative hypothesis; Sampling- Meaning and types of sampling; Probability and Non-Probability; Tools and

techniques of data collection- questionnaire, schedule, interview, observation, case study, survey etc. **(8 hours)**

Unit 3:REPORT WRITING AND ITS INTERPRETATION

Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports, Conclusions. **(8 hours)**

Unit 4:RESEARCH ETHICS AND SCHOLARY PUBLISHING

Ethics-ethical issues, ethical committees (human & animal); scholarly publishing- IMRAD concept and design of research paper, citation and acknowledgement, plagiarism and its concept and importance for scholar. **(8 hours)**

Unit 5: INTELLECTUAL PROPERTY RIGHT (IPR)

IPR- intellectual property rights and patent law, commercialization, New developments in IPR; copy right, royalty, trade related aspects of intellectual property rights (TRIPS); Process of Patenting and Development; Procedure for grants of patents, Patenting under PCT;Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. **(8 hours)**

Reference Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science &engineeringstudents""
2. WayneGoddardandStuartMelville,"ResearchMethodology:AnIntroduction"
3. RanjitKumar,2ndEdition,"ResearchMethodology:AStepbyStepGuideforbeginners"
4. Halbert,"ResistingIntellectualProperty",Taylor&FrancisLtd,2007.
5. Mayall,"IndustrialDesign",McGrawHill,1992.
6. Niebel,"ProductDesign",McGrawHill,1974.
7. Asimov,"IntroductiontoDesign",PrenticeHall,1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age",2016.
9. T.Ramappa,"IntellectualPropertyRightsUnderWTO",S.Chand,2008

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Low Power VLSI Design (VDT 304)

L:T:P::3:0:0 **Credits-3**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Improvise on the latest techniques used for designing power-efficient logic gates, latches, and flip-flops
2. Learn the latest MOS and bipolar models; breakthroughs in copper metallization, isolation and deep submicron processes; and new approaches to designing logic gates, latches, and flip-flops.

COURSE OUTCOMES (COs):

1. To understand the need for low power VLSI chips and basic analog and digital circuits suitable for low power design
2. To understand Gate-level Logic Simulation architectures and Probabilistic Power Analysis
3. To understand transistor Circuit and gate sizing issues
4. To understand Architecture and System level techniques for Power and Performance Management
5. To study Advanced Techniques for power reduction. To understand challenges involved in low power/voltage analog circuits and study of various techniques available

Course Contents:

UNIT-I Introduction to Needs for Low Power VLSI Chips, Charging and Discharging Capacitance, Short-circuit Current in CMOS Circuit, CMOS Leakage Current, Static Current, Basic Principles of Low Power Design, Low Power Figure of Merits, Gate-level Logic Simulation **(8 hours)**

UNIT-II Probabilistic Power Analysis of Random Logic Signals, Probability and Frequency, Probabilistic Power Analysis Techniques, Signal Entropy, Transistor and Gate Sizing, Transistor and Gate Sizing, Network Restructuring and Reorganization, Special Latches and Flip-flops, Low Power Digital Cell Library, Adjustable Device Threshold Voltage**(8 hours)**

UNIT-III Logical Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Precomputation Logic, Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM **(8 hours)**

UNIT-IV Power and Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits **(8 hours)**

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UNIT-V Challenges involved in low power Analog integrated circuits, issues about low supply voltage, roadmap, Techniques to design and implement low voltage/low power analog circuits like self cascode structure, flipped voltage follower, Bulk driven, FGMOS, QFGMOS etc.

(8 hours)

Reference Books:

1. Gary K. Yeap, , "Practical Low power Digital VLSI Design," Springer
2. Rabaey, Pedram, "Low power design methodologies," Kluwer Academic.
3. Kaushik Roy, SharatPrasad,"Low-Power CMOS VLSI Circuit Design," Wiley.
4. Christian Piguet, "Low-power CMOS circuits: technology, logic design and CAD tools," CRC Press, Taylor & Francis Group.

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System on Chip Design(VDT 305)

L:T:P::3:0:0 **Credits-3**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand the concepts of System on Chip Design methodology for Logic and Analog Cores
2. Understand the concepts of System on Chip Design Validation.
3. Understand the concepts of SOC Testing.

COURSE OUTCOMES (COs):

1. To analyze the functional and nonfunctional performance of the system early in the design process to support design decisions.
2. To analyze hardware/software tradeoffs, algorithms, and architectures to optimize the system based on requirements and implementation constraints.
3. Describe examples of applications and systems developed using a CO-design approach.
4. To appreciate issues in system-on-a-chip design associated with CO-design, such as intellectual property, reuse, and verification.

COURSE CONTENTs:

Unit-I System-level and SoC design methodologies and tools; **(8 hours)**

Unit-II HW/SW COdesign: analysis, partitioning, real-time scheduling, hardware acceleration; Virtual platform models, CO-simulation and FPGAs for prototyping of HW/SW systems. **(8 hours)**

Unit-III Transaction-Level Modeling (TLM) and Electronic System-Level (ESL) languages: System C. **(8 hours)**

Unit-IV High-Level Synthesis (HLS): allocation, scheduling, binding, resource sharing, pipelining; **(8 hours)**

Unit-V SoC and IP integration, verification and test. **(8 hours)**

Text Books/References:

1. Black, J. Donovan, System C: From the Ground Up, Springer, 2004.
2. P. Marwedel, Embedded System Design, Springer, 2006.

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VLSI Signal Processing(VDT-306)

L:T:P::3:0:0 **Credits-3**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand about DSP algorithms.
2. Explain about retiming techniques, folding and register minimization path problem.
3. Introduce abut algorithm strength reduction techniques & parallel processing of FIR and IIR filters.
4. Explain about finite word length effects and round off noise computation in DSP

Course Outcomes:

1. Ability to determine the parameters influencing the efficiency of DSP architectures and apply pipelining and parallel processing techniques to alter FIR structures for efficiency
2. Ability to analyze and modify the design equations leading to efficient DSP architectures for transforms apply low power techniques for low power dissipation
3. Ability to speed up convolution process and develop fast and area efficient IIR structures
4. Ability to develop fast and area efficient multiplier architectures
5. Ability to reduce multiplications and build fast hardware for synchronous digital systems

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UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS: Introduction to DSP systems – typical DSP algorithms, data flow and dependence graphs – criticalpath, loop bound, iteration bound, longest path matrix algorithm, pipelining and parallel processingof FIR filters, pipelining and parallel processing for low power. **(8 hours)**

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION: Retiming – definitions and properties, unfolding – an algorithm for unfolding, properties ofunfolding, sample period reduction and parallel processing application, algorithmic strengthreduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCTarchitecture, rank-order filters, Odd-Even, Merge-Sort architecture, parallel rank-order filters. **(8 hours)**

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS: Computer arithmetic techniques for low power system – reducing power consumption incombinational logic, sequential logic, memories – low power clock – advanced techniques –special techniques, adiabatic techniques – physical design, floor planning, placement and routing. **(8 hours)**

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES : Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-rippleand carry-save

multipliers, design of lyon‟s bit-serial multipliers using Horner‟s rule, bit-serialFIR filter, CSD representation, CSD multiplication using Horner‟s rule for precisionimprovement, Distributed Arithmetic fundamentals and FIR filters **(8 hours)**

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS WAVE AND ASYNCHRONOUS PIPELINING: Numerical strength reduction – sub-expression elimination, multiple constant multiplication,iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered singlephase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining - Bundled Dataversus Dual-Rail protocol. **(8 hours)**

REFERENCES

1. Keshab K. Parhi, “ VLSI Digital Signal Processing Systems, Design and Implementation “, Wiley, Interscience, 2007
2. U. Meyer – Baese, “ Digital Signal Processing with Field Programmable Gate Arrays”, Springer, 2nd Edition, 2004.

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Mixed Signa lIC Design(VDT 307)

L:T:P::3:0:0 **Credits-3**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand themixed signal circuits like DAC, ADC, PLL etc.
2. Gain knowledge on filter design in mixed signal mode.
3. Acquire knowledge on design different architectures in mixed signal mode

COURSEOUTCOMES(COs):

1. Todesignandperformanalysisoffundamentalbuildingblocksandbasicanalogcircuits.
2. tointroducecircuitdesignconceptsforbasicbuildingblocksusedinmixed-signalintegratedcircuitdesigns.
3. To provide a foundation for more complicated and advanced circuit designs
4. To handle both practical design and layout issues involved.

COURSECONTENT:

Unit-I Analog and discrete-time signal processing, analog integrated continuous-time and discrete-time filters, Analog continuous-time filters, passive and active filters, basics of analog discrete-time filtersandZ-transform **(8 hours)**

Unit-II

Switched-capacitor filters, Non-idealities in switched-capacitor filters, switched capacitor filter architectures, switched capacitor filter applications, **(8 hours)**

Unit-III

Basics of data converters, Successive approximation ADCs, Dual slope ADCs ,Flash ADC, Pipeline ADC **(8 hours)**

Unit-IV

Hybrid ADC structures, higher solution ADC, DAC, Mixed signal layout, Inter connects and data transmission,Voltage-modesignalinganddatatransmission,Current-modesignalinganddatatransmission. **(8 hours)**

Unit-V

Introduction to frequency synthesizers and synchronization, basics of PLL, Analog PLL, Digital PLL, Delay Locked Loop(DLL). **(8 hours)**

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Text Books/References:

1. R.Jacob Baker, "CMO Smixed-signalcircuitdesign",WileyIndia, IEEE press, reprint2008.
2. BehadRazavi,"Design of analog CMOS integrated circuits", McGraw-Hill,2003

3. R.Jacob Baker,"CMOS circuit design, layout and simulation" Revisedsecondedition,IEEEpress,2008.

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Memory Technologies(VDT-308)

L:T:P::3:0:0 **Credits-3**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Acquire knowledge about different types of semiconductor memories.
2. Study about architecture and operations of different semiconductor memories.
3. Comprehend the low power design techniques and methodologies

COURSEOUTCOMES(COs):

1. Analysis the different types of RAM, ROM designs.
2. Analysis the different RAM and ROM architecture and interconnects.
3. Analysis about design and characterization technique.
4. Analysis of different memory testing and design for testability.
5. Identification of new developments in semiconductor memory design.

Course Content:

UNIT 1

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs; DRAMs, MOS DRAM Cell, BiC MOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM. **(8 hours)**

UNIT 2

Non-Volatile Memories: High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. **(8 hours)**

UNIT 3

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM Fault Modeling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing. **(8 hours)**

UNIT 4

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing. **(8 hours)**

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UNIT 5

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc. **(8 hours)**

Reference Books:

1. Ashok K. Sharma, “Semiconductor Memories: Technology, Testing and Reliability",
1. Prentice- Hall of India Private Limited.
2. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and
3. Applications”, Wiley Interscience Publication.
4. Wen C. Lin, “Handbook of Digital System Design”, CRC Press.
5. KiyooItoh, “VLSI memory chip design”, Springer International Edition.
6. Chenming C Hu, “Modern Semiconductor Devices for Integrated Circuits”, Prentice Hall.

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HARDWARE SOFTWARE CO-DESIGN FOR FPGA (VDT-309)

L:T:P::3:0:0 **Credits-3**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Analyzing the control-flow and data-flow of a software program and a cycle-based hardware description
2. Partitioning simple software programs into hardware and software components, and creating appropriate hardware-software interfaces to reflect this partitioning
3. Identifying performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software component

Course Outcomes:

1. Describe The Broad Range of System Architectures and Design Methodologies that currently exist and define their fundamental attributes.
2. Discuss the Dataflow Models as a State-of-the-Art Methodology to Solve Co-Design Problems and to Optimize the balance between Software and Hardware.
3. Understand in Translating between Software and Hardware Descriptions through Co-Design Methodologies.
4. Understand the State-of-The-Art practices in developing Co-Design Solutions to problems using modern Hardware/Software Tools for building prototypes.
5. Understand the Concurrent Specification from an Algorithm, Analyze its behavior and partition the Specification into Software (C Code) and Hardware (HDL) Components

Couse Content:

UNIT I SYSTEM SPECIFICATION AND MODELLING: Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification andModeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor
Architectures with One ASIC, Single-Processor Architectures with Many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification. **(8 hours)**

UNIT II HARDWARE/SOFTWARE PARTITIONING : The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation ofThe Partitioning Graph, Formulation of The

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HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms. **(8 hours)**

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS: The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis. **(8 hours)**

UNIT IV PROTOTYPING AND EMULATION : Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments,Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems. **(8 hours)**

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-Simulation. **(8 hours)**

REFERENCE BOOKS:

1. Patrick Schaumont, “A Practical Introduction to Hardware/Software Co-design”, Springer,2010.
2. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Publisher, 1998.
3. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Publisher,1997.
4. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design”, Kaufmann Publisher,2001.

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FPGA System Design (VDT-310)

L:T:P::3:1:0 **Credits-4**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Learn and use design flow for using FPGA.
2. Learn programming of FPGA with practical circuits
3. Design for higher performance or lower area using alternative circuit families.

Course Outcomes:

1. Describe the architecture of FPGAs and logic design process and implement different logic circuits on the internal architecture of FPGA
2. Write HDL codes of combinational and sequential Circuits and perform their functional verification
3. Design the control unit of a Digital Circuit and implement it using Finite State Machines (FSMs).
4. Design of efficient and high speed adders and multipliers for optimizing the datapath of digital circuits.
5. Analyze Digital design in terms of area, power and speed.

Course Contents:

UNIT-I Introduction: Different kinds of programmable logic devices: Field Programmable Gate Array (FPGA), Programmable Logic Device (PLD), FPGA manufacturers (Xilinx, Altera, Actel, Lattice Semiconductor, Atmel). FPGA applications. Adjoining devices. Instruments and software. **(8 hours)**

UNIT-II The Structure of FPGA: FPGA general description. Different kinds of FPGA packages. FPGA architecture. Internal hard modules of FPGA (CLB, Block RAM, DCM), their meanings and usage. Different kinds of I/O modules, their usage and configuration. FPGAs Field

Programmable Gate Arrays–Logic blocks, routing architecture, Design flow,Technology Mapping for FPGAs. **(8 hours)**

UNIT-III FPGA Design Flow: Architecture design. Project design using Verilog Hardware Description Language (HDL). Defining testing methodology and test bench design. RTL simulation, synthesizing, implementation, gate level simulation of design. Reusing of internal hard modules during design and implementation. **(8 hours)**

UNIT-IV Testing Methodology: Functional and gate level testing. SDF file description and usage. **(8 hours)**

UNIT-VFPGA Configuration: Different types of FPGA configuration files. Generation of configuration file and its loading into FPGA. **(8 hours)**

Reference Books:

1. Scott Hauckand Andre Dehon. Reconfigurable Computing: The Theory and Practice of FPGABased Computation.
2. P.K.Chan& S. Mourad, Digital Design using Field ProgrammableGate Array, Prentice Hall.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology,Kluwer Academic Pub.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
4. V. Sklyarov, L. Skliarova, A. Barkalov, L. Titarenko. Synthesis and Optimization of FPGA- Based Systems. Springer; 2014

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VLSI CIRCUIT DESIGN(VDT-311)

L:T:P::3:1:0 **Credits-4**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Learn digital CMOS logic design.
2. Realize importance of testability in logic circuit design.
3. Overview SoC issues and understand PLD architectures with advanced features.

COURSE OUTCOMES:

At the end of the course the student will be able to:

1. To get acquainted with basic theory of MOS transistors and familiar with CMOS fabrication technology
2. To understand the concepts related to implementation of Combinational CMOS logic circuits
3. To understand the concepts related to implementation of sequential CMOS logic circuits
4. To understand the concepts of memories design with efficient architectures to improve access times, power consumption.
5. To understand the process behind testing of CMOS integrated circuits

UNIT 1: REVIEW OF MOSFET OPERATION AND CMOS PROCESS FLOW: MOS Threshold voltage, MOSFET I-V characteristics: Long and short channel, MOSFET capacitances, lumped and distributed RC model for interconnects, SPICE Model, CMOS process flow, Layout and design rules. **(8 hours)**

UNIT 2: CMOS INVERTER ANDCOMBINATIONAL LOGIC: The CMOS Inverter, CMOS Logic Gates: NAND Gate, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers, adders, Complex logic circuit. **(8 hours)**

UNIT 3: SEQUENTIAL LOGIC: Behaviour of Bistable element, monostable and a stable circuits, Static latches and flip-flops (FFs), dynamic latches and FFs, Voltage Bootstrapping, Synchronous dynamic high Performance dynamic CMOS circuits. **(8 hours)**

UNIT 4: MEMORIES AND ARRAY STRUCTURES: MOS-ROM, SRAM cell, memory peripheral circuits, signal to noise ratio, power dissipation. **(8 hours)**

UNIT 5: **Testing, Debugging, and Verification:** Test vectors, Fault Models, Observability, Controllability, Repeatability, Survivability, Fault Coverage, Automatic Test Pattern Generation (ATPG),Delay Fault Testing, Ad Hoc Testing, Scan Design, Built-In Self-Test (BIST), IDDQ Testing, Design for Manufacturability, Boundary Scan etc. **(8 hours)**

BOOKS :

1. Rabaey, Chandrakasan and Nikolic, “Digital Integrated Circuit: A Design Perspective”, PHI; Latest Edition.
2. Sung-Mo Kang, Yusuf Liblebici, “CMOS Digital Integrated Circuits,” Tata Mc Graw Hill.
3. Weste and Eshraghian, “Principles of CMOS VLSI Design” Addison Wesley, Latest Edition
4. Weste and Harris, “CMOS VLSI Design”
5. Ajit Pal, ―Low-Power VLSI Circuits and Systems‖, Springer, 2015.
6. K. Roy and S. C. Prasad, ―Low-Power CMOS VLSI Circuit Design‖, Wiley, 2000.

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Embedded System Design(VDT-312)

L:T:P::3:1:0 **Credits-4**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Acquire knowledge about the basic functions, structure, concepts and applications of embedded systems
2. Learn the method of designing and program an Embedded Systems for real time applications
3. Acquire knowledge about the development of embedded software using RTOS and implement small programs to solve well-defined problems on an embedded platform.

COURSE OUTCOMES (COs):

CO1: To develop basic understanding of embedded systems in general and their applications.
CO2: To comprehend the architecture and components of embedded systems.
CO3: To understand the onboard and external communication interfaces.
CO4: To understand the concepts of multiprocessing, multitasking and shared memory.

COURSE CONTENTs:

Unit I

Formal definition of an Embedded System. Embedded system examples. Compare and contrast embedded system and conventional/generic computer system. Overview of elements of an Embedded system. Processor level implementation using (a) generic devices (b) full custom ASIP and (c) Soft core implementation on FPGA. Key parameters of Embedded System Design (Time to market and cost). **(8 hours)**

Unit II

Microcontroller Classification based on memory access, ISA, data bus width. Example microcontroller families (8-bit, 16-bit and 32-bit examples). Memory technologies, Memory interface busses. Desirable microcontroller features. Development, debugging and testing tools. Elements of Microcontroller ecosystem: Reset, Clock, Power supply and program download options. **(8 hours)**

Unit III

AVR Microcontroller architecture details. Elements of physical interfacing: Input devices, Output, environmental sensors, actuators. Elements of analog signal processing. Inter and Intra-device communication Interfaces. Real Time Clock. Storage devices. Power supply topologies for embedded systems. **(8 hours)**

Unit IV

Elements of Embedded C programming; pointers and memory optimization, bit-wise operations, using and creating device library, Compiler optimization. Interrupt driven programming and Foreground-background programming model. **(8 hours)**

Unit V

Introduction to RTOS. Threads, Processes and Message Passing. Basics of scheduling. Complete system design example. Security in embedded systems. System testing and debugging. **(8 hours)**

Text Books:

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1. Embedded System Design: Embedded Systems Foundation of Cyber-Physical Systems and the Internet of Things. 3rd Edition. Peter Marwedel. ISBN 978-3-319-56043-4. Springer.
2. Embedded Hardware: Know It All. Jack Ganssle et al. ISBN: 0750685840. Newnes.
3. Designing Embedded Hardware. 2nd Edition. John Catsoulis. ISBN: 0596007558. O'Reilly
4. Embedded Systems: World Class Designs. Jack Ganssle. ISBN: 0750686251. Newnes.

Testing of VLSI Circuits(VDT-313)

L:T:P:: 3:1:0 **Credits-4**

COURSE OBJECTIVES:

From this course, students will be able to:

Deal with the study of VLSI design flow, Functional verification, verification flow, need of electronic testing, fault modeling, test generation for combinational circuits

COURSE OUTCOMES (COs):

1. Study of test generation for sequential circuits, fault simulation.
2. Study of Built-In Self-Test (BIST), Memory testing, Design for Testability (DFT)
3. Study of SoC test, fault diagnosis, Analog/RF tests.

Course Contents:

UNIT I - BASICS OF TESTING AND FAULT MODELING (8 hours)

Introduction- Principle of testing - types of testing - DC and AC parametric tests - fault modeling- Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation

UNIT II - TESTING AND TESTABILITY OF COMBINATIONAL CIRCUITS (8 hours)

Test generation basics - test generation algorithms - path sensitization - Boolean difference – Dalgorithm– PODEM - Testable combinational logic circuit design.

UNIT III - TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS (8 hours)

Testing of sequential circuits as iterative combinational circuits - state table verification - test generation based on circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) - partial scan - Boundary scan

UNIT IV - MEMORY, DELAY FAULT AND IDDQ TESTING (8 hours)

Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults –Delay test- IDDQ testing - testing methods - limitations of IDDQ Testing

UNIT V - BUILT-IN SELF-TEST (8 hours)

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Test pattern generation of Built-in Self-Test (BIST) - Output response analysis – BIST architectures.

Reference Books:

1. P. K. Lala, “Digital Circuit Testing and Testability”, Academic Press.

2. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers.

3. N.K. Jha and S.G. Gupta, “Testing of Digital Systems”, Cambridge University Press.

4. ZainalabeNavabi, “Digital System Test and Testable Design: Using HDL Models and Architectures”, Springer.

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ASIC DESIGN USING VERILOG(VDT-314)

L:T:P:: 3:1:0 **Credits-4**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand how modern digital systems are designed based around the use of hardware description languages, logic synthesis and mapping onto standard cell and field programmable logic.
2. Understand non-logic-design issues in ASIC design, including timing, power, and verification.
3. Know how to approach block level optimization in ASIC design.

COURSE OUTCOMES:

At the end of the course, the student will be able to:

1. Explain VLSI design flow using HDL.
2. Design the combinational and sequential digital systems.
3. Employ EDA tools to model a digital system.
4. Write test benches to verify the design.

Course Contents:

UNIT 1: INTRODUCTION TO VLSI AND CAD TOOLS: Evolution of CAD, emergence of HDLs, typical HDL-based design flow, Verilog HDL. Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, simulation and synthesis, system task, test bench, programming language interface, simulation and synthesis tools. **(8 hours)**

UNIT 2: LANGUAGE CONSTRUCT AND CONVENTION IN VERILOG: Introduction, keywords, identifiers, white space characters, comments, numbers, strings, logic value, strengths, data type, scalars and vectors, parameters, memory, operators.
Gate-Level Modeling: Introduction, module structure, design of flip-flops with gate primitives, delays, net types. **(8 hours)**

UNIT 3: DATAFLOW LEVEL MODELING: Introduction, Continuous assignments structure, delays and continuous assignments, assignment to vectors, operators.
BEHAVIORAL MODELING: Introduction, operations and assignments, initial construct, always construct, assignment with delay, wait construct, blocking and non-blocking assignment, assign-deassign construct, for loop, while loop, force-release construct, parallel blocks.
(8 hours)

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UNIT 4: TASKS AND FUNCTIONS DESIGN: Introduction, function, structure and scope of function, task enabling, user defined primitive: combinational and sequential user defined primitive, path delay, system task and functions, file based task and function. **(8 hours)**

UNIT 5: QUEUES AND FINITE STATE MACHINE: Introduction, task for queue initialization, task for adding and removing from the queue, design of finite state machine: Moore machine and Mealy machine. **(8 hours)**

BOOKS:

3. Samir Palnitkar, "Verilog HDL, A Guide to Digital Design and Synthesis", Second Edition, Pearson Education, 2004
4. T.R. Padmanabhan, B. Bala Tripura Sundari "Design through Verilog HDL" Wiley India Pvt. Ltd, 2008
3. J. Bhaskar, "Verilog HDL Synthesis", BS publications, 2001.

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Algorithms for VLSI Design Automation(VDT-315)

L:T:P:: 3:0:0 **Credits-3**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand techniques for electronic design automation (EDA), a.k.a. computer-aided design (CAD)
2. Study IC technology evolution and their impacts on the development of EDA tools

COURSE OUTCOMES:

1. Understand the basic concept of VLSI .
2. Differentiate analog and digital VLSI design cycle.
3. Apply appropriate automation algorithms for partitioning, floor planning, placement and routing.
4. Design clock trees to distribute the clock signals on the chip while satisfying various. constraints like clock skew and wire length.

Course Contents:

UNIT 1: VLSI physical design automation and Fabrication VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices **(8 hours)**

UNIT 2: VLSI automation Algorithms Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing. **(8 hours)**

UNIT 3: Floor planning & pin assignment: Problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block& cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment Placement Problem formulation, classification of placement algorithms, simulation base placement algorithms, recent trends in placement **(8 hours)**

UNIT 4: Global Routing and Detailed routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms. **(8 hours)**

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UNIT 5: Over the cell routing & via minimization: Two layers over the cell routers, constrained & unconstrained via minimization **Compaction:** Problem formulation, classification of compaction algorithms, One dimensional compaction, two dimension based compaction, hierarchical compaction. **(8 hours)**

Reference Books :

1. NaveedShervani, "Algorithms for VLSI physical design Automation", KluwerAcademic Publisher, Second edition.
2. ChristophnMeinel& Thorsten Theobold, "Algorithm and Data Structures for VLSIDesign", Kluwer Academic Publisher.
3. R. Drechsler, "Evolutionary Algorithm for VLSI CAD", Kluwer Academic Publication.

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Sensors and Actuators(VDT-316)

L:T:P:: 3:0:0 **Credits-3**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Understand the operation of commonly employed sensors and actuators
2. Be able to analyze and select the most appropriate sensors or actuator for an application.
3. Be able to design and construct the appropriate interface circuits for the sensors and actuators.

COURSE OUTCOMES (COs):

1. Interpret physical principles applied in sensors and actuators
2. To model and design sensors with desired physical and chemical properties
3. Identify various types of sensors including thermal, mechanical, electrical, electromechanical and optical sensors
4. To implement sensors for physical, chemical, and biochemical applications

Course Contents:

Unit-I Sensors/Transducers: Principles – Classification – Parameters Characteristics – Environmental Parameters (EP) – Characterization Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor Types- Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors **(8 hours)**

Unit-II Thermal Sensors: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors **(8 hours)**

UNIT-III Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors –Anisotropic Magneto resistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors –Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros –Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors Radiation Sensors: Introduction – Basic Characteristics – Types of Photo sensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors. **(8 hours)**

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UNIT-IV Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential – Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– References Electrodes - Sensor Electrodes – Electro ceramics in Gas Media . Smart Sensors: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation Sensors – Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors –– Sensors for Manufacturing –Sensors for environmental Monitoring **(8 hours)**

UNIT-V Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors. **(8 hours)**

Reference Books:

1. D. Patranabis – “Sensors and Transducers” –PHI Learning Private Limited.
2. W. Bolton – “Mechatronics” –Pearson Education Limited.

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Design for Testability(VDT-317)

L:T:P::3:0:0 **Credits-3**

COURSE OBJECTIVES:

From this course, students will be able to:

1. Apply the concepts in testing which can help them design a better yield in IC design
2. Tackle the problems associated with testing of semiconductor circuits at earlier design levels
3. Identify the design for testability methods for combinational & sequential CMOS circuits

COURSE OUTCOMES (COs):

CO1: To understand types of faults and also to study about fault detection
CO2: To understand the concepts of the test generation methods.
CO3: To understand the fault diagnosis methods will learn testing and verification in VLSI design process
CO4: To understand Automatic test pattern generation concepts for combinational and sequential circuits
CO 5: To perform memory test, defect screening, SOC testing etc

COURSE CONTENTs:

Unit-I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault. **(8 hours)**

Unit-II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG. **(8 hours)**

Unit-III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan. **(8 hours)**

Unit-IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

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(8 hours)

Unit-V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions. **(8 hours)**

Text Books/References:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits- M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.
2. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
3. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

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Technical Writing and Presentation Skills (AHT-303)

L:T:P::2:0:0 **Non-credits**

Course Objectives:

- To develop effective writing and presentation skills in students.
- To develop textual, linguistic and presentation competencies in students appropriate for their professional careers.

Course Outcomes:

After the successful completion of course, the students will be able to:

CO1: Write clearly and fluently to produce effective technical documents.

CO2: Demonstrate an appropriate communication style to different types of audiences both orally and written as per demand of their professional careers.

CO3: Communicate in an ethically responsible manner.

Course Contents:

WRITING SKILLS

Unit-I **(4 hours)**

Technical Writing-Basic Principles: Words-Phrases-Sentences, Construction of Cohesive Paragraphs, Elements of Style.

Unit-II **(4 hours)**

Principles of Summarizing: Abstract, Summary, Synopsis

Unit-III **(6 hours)**

Technical Reports: Salient Features, Types of Reports, Structure of Reports, Data Collection, Use of Graphic Aids, Drafting and Writing

PRESENTATION SKILLS

Unit-IV **(6 hours)**

Speaking Skills: Accuracy vs. Fluency, The Audience, Pronunciation Guidelines, Voice Control.

Unit-V **(8 hours)**

Professional Presentations: Planning, Preparing, Presentation Strategies, Overcoming, Communication Barriers, Using Technology, Effective Presentations.

References:

1. Kumar, Sanjay &PushpLata, “Communication Skills”, Oxford UniversityPress,2011.
2. Quirk & Randolph, “A University Grammar of English”, Pearson,2006.
3. Rutherford, Andrea J., “Basic Communication Skills for Technology”, Pearson 2007.
4. Rizvi, M Ashraf, “Effective Technical Communication”, McGraw Hill,2009.
5. Leigh, Andrew & Maynard, Michael, “The Perfect Presentation”, Random House.

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6. Barker, Larry L., “Communication”, Prentice-Hall.
7. Lesikar & Flatley, “Basic Business Communication-Skills for Empowering the Internet Generation”, Tata McGraw-Hill.