वीर माधो सिंह भण्डारी उत्तराखण्ड प्रौद्योगिकी विश्वविद्यालय

(उत्तराखण्ड सरकार द्वारा अधिनियम 415/2005 द्वारा स्थापित पूर्ववर्ती उत्तराखण्ड तकनीकी विश्वविद्यालय)

Veer Madho Singh Bhandari Uttarakhand Technical University

(Formerly Uttarakhand Technical University Established University by Act no.415/2005by Uttarakhand Government)

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पत्रांक : 831 /वी0मा0सि0भ0उ0प्रौ0वि0वि/2024 Date- 07/06/24

सेवा मे,

निदेशक
विश्वविद्यालय के कैम्पस व समस्त सम्बद्ध संस्थान,
वी0मा0सि0भ0उ0प्रौ0वि0वि देहरादून।

विषयः– Faculty Training on "Semiconductor and ESDM Domain " के संबंध में।

महोदय,

अवगत कराना है कि विश्वविद्यालय में स्थापित एकेडमिक स्टॉफ डेवलपमेन्ट सेन्टर के तत्वाधान में दिनाक 01 से 06 जुलाई, 2024 के मध्य एक सप्ताह की FDP on Semiconductor and ESDM Domain को आयोजित किया जा रहा है। अपनी संस्था में उपलब्ध शिक्षको (ECE, EE, EEE विभागो से) में कम से कम दो शिक्षकों को आवश्यक रूप से प्रतिभाग कराने का कष्ट करें।

संलग्नक

कुलसचिव

Veer Madho Singh Bhandari Uttarakhand Technical University
Dehradun (Uttarakhand) - INDIA

Academic Staff Development Centre

Organizes

One week Teacher's Training Program for faculty members of Affiliated / Campus Institutions

On

"Semiconductor and ESDM Domain"

Objective: Teacher's training program aims at development of teachers serving in affiliated / campus institutions of the Veer Madho Singh Bhandari Uttarakhand Technical University. Every participant will be provided with a certificate of participation after the successful completion of the program by the individual.

Eligibility: Teachers serving in the affiliated / campus institutions of Veer Madho Singh Bhandari Uttarakhand Technical University are eligible to participate in the training program.

Seats and Fees: There are only 30 seats in the program and the admission will be offered on first come first serve basis. A registration fee of Rs. 300/- is to be paid by the teachers in the training program by the due date of registration by filling a Registration form and getting it forwarded by their respective Director of the institute. Participant will be provided the registration kit and working lunch during the programme. No TA/DA shall be paid to participants. Also, no arrangements for stay will be made for participants. The University reserves the right to accept or reject any candidature at any stage. A certificate of participation will be given to all the participants who will be attending all sessions of the programme.

Agenda for cadence sessions

Session-1:

- Introduction to Semi-Custom IC Design Flow
- Cadence Solutions for Semi-Custom IC Design
- Functional Verification using Incisive
- RTL Synthesis using Genus Synthesis Solution

Session-2:

- Physical Implementation using Innovus that includes
  - Floor Planning ✓ Power Planning ✓ Placement ✓ CTS ✓ Routing
- Timing Analysis
- Power Analysis
- Parasitic Extraction
- Generation of GDSII

Session-3:

- Introduction to Full Custom IC Design Flow
- Cadence Solutions for Custom IC Design
- Schematic Capture using Virtuoso Schematic Editor
- Symbol Creation
- Testbench Creation using Virtuoso Schematic Editor
- Functional Simulation using Spectre

Session-4:

- Layout Design using Virtuoso Layout Editor
- Physical Verification which includes DRC & LVS
- Parasitic Extraction using Quantus
- Post Layout Simulation
- Generation of GDSII

Other Topics

1.0 – Electronic Product Design Cycle

2.0 – Design Entry (Schematic): Design Example – Hands On

3.0 – Predict the behavior of your circuit: Circuit Simulation – Hands On

4.0 – Generate the BOM (Bill of Material)

5.0 – Route the Layout

6.0 – Generate Fabrication Files/Data for Layout

7.0 – Generate 3D View of Layout and MCAD Interface: - Demo

8.0 PCB Fabrication demo Using MITS PCB prototyping System.

Registration link :

Registration link for the FDP is following.

https://online.uktech.ac.in/ums/Student/Public/DevelopmentRegistration

Please use the enclosed registration for submission of the candidature.

Last Date for the registration is 28-06-2024.

Academic Staff Development Centre
Veer Madho Singh Bhandari Uttarakhand Technical University
Dehradun (Uttarakhand) - INDIA

REGISTRATION FORM

Three Days Teacher's Training Program for faculty members of Affiliated / Campus Institutions

On

Semiconductor and ESDM Domain

Name:
Designation:
Department:
Institute Name:
Correspondence Address:
Mobile No:
Email Address:
Teaching Experience in years:
Forwarding by the employer Institute:

The institute has no objection to the participation of aforesaid faculty member for participating in the Faculty Development Programme organized by Academic Staff Development Centre of VMSB Uttarakhand Technical University, Dehradun for the duration mentioned above.

Signature and Seal of Director/ Principal of Institute
Name of institute:
Date:

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Venue of the program :

Pt. Narayan Dutt Tiwari Conference Hall, Administrative Building of Veer Madho Singh Bhandari Uttarakhand Technical University, Dehradun.