Sub Code: VDT-301	**ROLL NO.**

Model Question Paper

COURSE: M.TECH	**BRANCH**: VLSI DESIGN
SEMESTER: 3 .	**SUBJECT**: CMOS ANALOG CIRCUIT DESIGN
Duration: 3:00 hrs	**Max marks: 100**

Note: Attempt all questions.

1. **Attempt any two parts of the following question.** **5x4 = 20**

   A. Give the relative doping levels of the emitter, base and collector for the vertical npn transistor?

   B. Which of the parasitic bulk resistances (R_E, R_B, and R_C) for a lateral pnp transistor, is usually the largest? Smallest?

   C. What is the purpose of the n+ buried layer? Explain with justification.

   D. Show that MOSFET acts as a controlled resistor in deep triode region.

   E. What is the effect of channel length modulation in the basic current mirror circuit?

   F. Discuss the temperature dependence of saturation drain current in MOSFETs.

2. **Attempt any two parts of the following question.** **20**

   A. Discuss how the effect of channel length modulation is suppressed in a cascode current mirror.

   B. Describe the frequency response of a common source amplifier with necessary equivalent circuits and hence calculate the input impedance and output impedance of the amplifier.

   C. Explain the concept of push-pull inverter with neat diagram. Derive the small signal voltage gain and find the zero in plane.

3. **Attempt any two parts of the following question.** **20**

   A. Explain the following terms with neat sketch.
   i) Switched capacitor comparators.
   ii) Regenerative comparators.

   B. Choose values of VGS = 1,2,3,4 and 5V, assume that the channel modulation parameter is zero. Sketch to scale the output characteristics of an enhancement n-channel device if $V_T = 0.7V$ and $I_D = 500\mu A$ when $V_{GS} = 5\ V_{in}$ saturation.

C. Draw the schematic of 4 bit resistor based binary weighted D/A converter and explain it operation. What are the advantages of binary weighted converters?

4. **Attempt any two parts of the following question.** **20**

A. Find the numerical values of all roots and the mid-band gain of the transfer function v_{out}/v_{in} of the differential amplifier shown in Figure 1. Assume that K_N' = 110μA/V2, V_{TN} = 0.7V, and λ_N = 0.04V^{-1}. The values of Cgs = 0.2pF and Cgd = 20fF.

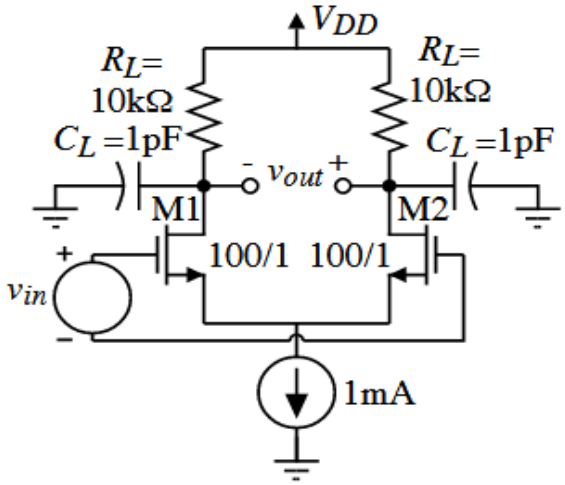

Figure.1

B. With neat sketch and necessary equations explain the concept of nulling resistor compensation of two stage CMOS Op-Amp.

C. Describe how the small-signal voltage gain of a differential amplifier can be computed by applying: (i) principle of superposition, and (ii) concepts of virtual ground and half circuit.

5. **Attempt any two parts of the following question.** **20**

A. Describe the circuit of a differential pair including the input-referred noise sources and hence estimate the input-referred noise, by modeling the noise sources as: (i) voltage sources, and (ii) current sources.

B. Compare the dynamic latch with the NMOS and PMOS latches. What are the advantages and disadvantages of the two latches?

C. A simple first-order filter is to be built with a polysilicon resistor and a MOS capacitor. The polysilicon resistor has a sheet resistance of 50/sq. ± 30% and is 5m wide. The MOS capacitor is

2fF/m2 ± 10%. The -3dB frequency of the low-pass filter is 1MHz.
(i.) Choose the size of the resistor (the number of squares, N) to minimize the total area of the filter including both the resistor and the capacitor. Find the area of the resistor and the capacitor in m2 and their values.
(ii.)Using the worst-case tolerance of the resistor and capacitor, find the maximum and minimum -3dB frequencies.