Course Name: Computer Organization & Architecture

Course Outcomes (COs):

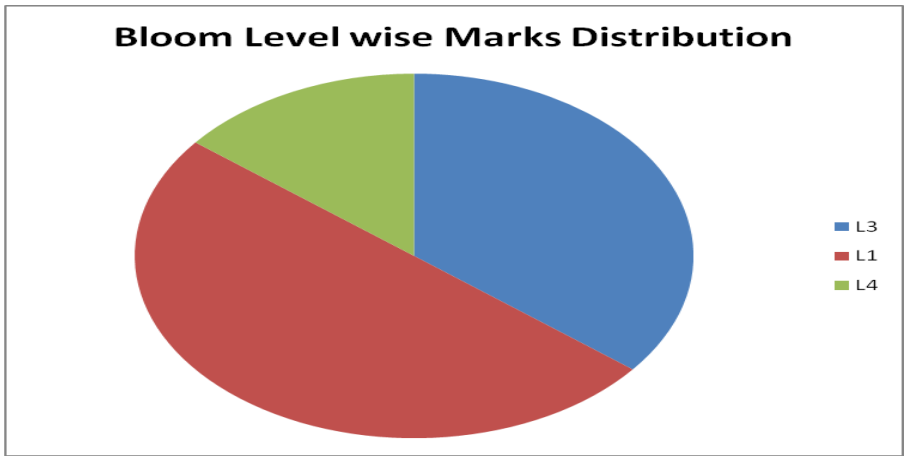
At the end of the course the student should be able to:

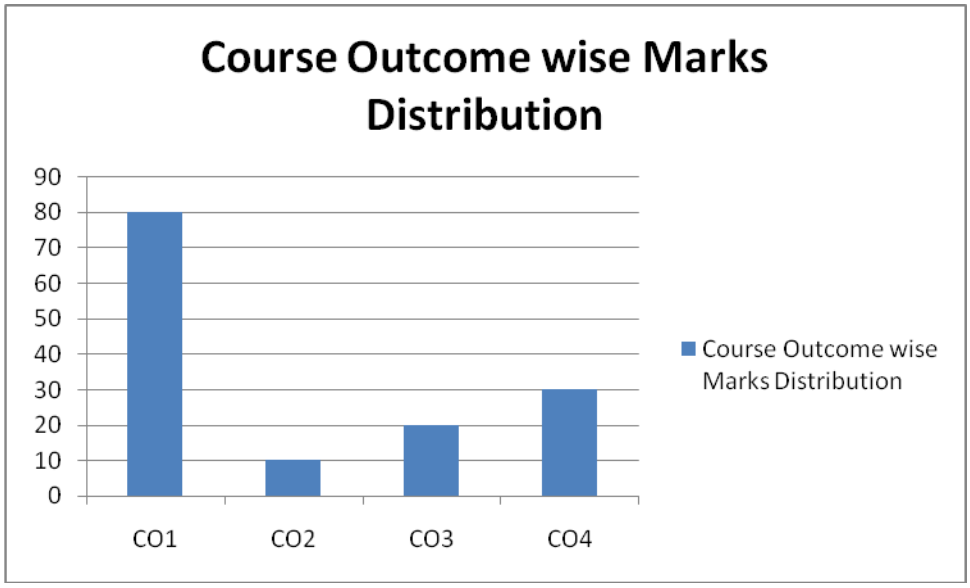
1. Understand the basic organization of computer and different instruction formats and addressing modes
2. Analyze the concept of pipelining, segment registers and pin diagram of CPU.
3. Understand and analyze various issues related to memory hierarchy
4. Evaluate various modes of data transfer between CPU and I/O devices and Examine various inter connection structures of multi processors.

Model Question Paper for End Semester Examination					
Course Code:CAT007		**Course Title: Computer Organization and Architecture**			
Duration: 3 hrs		**Max. Marks: 100**			
Note: Answer five questions; any Four questions from each unit-I and unit-II and Two full question from unit-III, IV & V					
Unit-I					
Q.No	Questions	Marks	CO	PI Code	B L
1 a	Convert the decimal number 205.5 to base 3, base 4, base 7 base 8 and base 16.	5	CO1	1.4.4	L3
b	Perform the subtraction with the following decimal number using- i. 10's complement ii. 9's complement check the answer by straight subtraction- a. 5250 - 321 b. 753 - 864	5	CO1	1.4.4	L3
c	simplify the following Boolean function using 4- variable maps- i. F(A,B,C,D) = ∑ (4 , 6 , 7 , 15) ii. F(A,B,C,D) = ∑ (3 , 7 , 11 , 13 , 14 , 15)	5	CO1	1.4.4	L3
d	Why NAND gate and NOR gate is called Universal gate ?	5	CO1	1.4.4	L1

e	Simplify the Boolean function- f (A,B,,D)=∑(0,2,3,5,7,8,9) WITH (10,11,12,13,14,15) As don't cares.	5	CO1	1.4.4	L3
	Unit-II				
2a	Draw and explain a 4 - bit parallel binary Subtractor.	5	CO1	1.4.4	L1
b	Realize a full adder using NAND gates only.	5	CO1	1.4.4	L1
c	Realize a Carry look ahead adder.	5	CO1	1.4.4	L1
d	Draw two bit Magnitude comparator.	5	CO1	1.4.4	L1
e	What is Multiplexer. Draw 4x1 MUX.	5	CO1	1.4.4	L1
	Unit-III				
a	Show that a JK flip flop can be converted to a D flip flop with an inverter between the J and K input.	10	CO1	1.4.4	L2
b	Design a 3 bit binary counter.	10	CO1	1.4.4	L1
c	Design a Johnson counter.	10	CO1	1.4.4	L1
	Unit-IV				
a	Draw a timing diagram of SC is cleared to 0 at time T_3 if control signal C7 is active. C_7T_3: SC<-0 C_7 is activated with the positive clock transition associated with T.	10	CO4	2.1.2	L4
b	The content of AC in the basic computer is hexadecimal A937 and the initial value of E is 1. Determine the content of AC,E,PC,AR and IR in hexadecimal after the execution of the CLA instruction. The initial value of PC is hexadecimal 021.	10	CO2	2.1.2	L4
c	A stack organization such that SP always points at the next empty location on the stack. This means the SP can be initialized to 4000 and the firt item in the stack is stored in location 4000. List the micro operation for the PUSH and POP operation.	10	CO4	1.4.4	L3

Unit-V					
a	Consider a cache consisting of 256 blocks of 8 words each, for a total of 2048 words, and assume that the main memory is addressable by a 16-bit address. The main memory has 64K words which are divided into 8192 blocks of 8 words each. Find the number of bits in Tag, Block and Word Field of the main memory address for direct mapping scheme.	10	CO3	1.4.4	L3
b	Write a note on memory hierarchy with the neat diagram.	10	CO3	1.4.4	L1
c	Describe the Direct Mapping.	10	CO3	1.4.4	L1





BL – Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 – Applying, 4 – Analysing, 5 – Evaluating 6 - Creating)

CO – Course Outcomes

PO – Program Outcomes;

PI Code – Performance Indicator Code

Competency addressed in the Course and corresponding PerformanceIndicators

Competency	Performance Indicators
1.4: Demonstrate competence in computer science engineering knowledge	**1.4.4** Apply machine dependent/independent features to build system modules.
2.1: Demonstrate an ability to identify and characterize an engineering problem.	**2.1.2**: Identify processes, modules, variables, and parameters of computer based system to solve the problems.

Eg: 1.2.3: Represents Program Outcome „1", Competency „2" and Performance Indicators „3".